

# MC68HC05RC9 MC68HC05RC18

## General Release Specification

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## Section 1. General Description

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## 1.2 Introduction

The MC68HC05RC18 is a general-purpose, low-cost addition to the M68HC05 Family of microcontroller units (MCUs) and is suitable for remote control applications. It contains the HC05 central processing unit (CPU) core, including the 14-stage core timer with real-time interrupt (RTI) and computer operating properly (COP) watchdog systems. On-chip peripherals include a carrier modulator transmitter (CMT). The 16-Kbyte memory map has 15,936 bytes of user ROM and 352 bytes of RAM. There are 20 input-output (I/O) lines (eight having keyscan logic and pullups) and a low-power reset pin. The MC68HC05RC18 is available in a 28-pin small outline integrated circuit (SOIC) package, a 29-pin dual-in-line package (DIP), or a 44-pin plastic leaded chip carrier (PLCC). Four additional I/O lines are available for bond out in higher pin count packages.

## 1.3 Features

Features of the MC68HC05RC18 include:

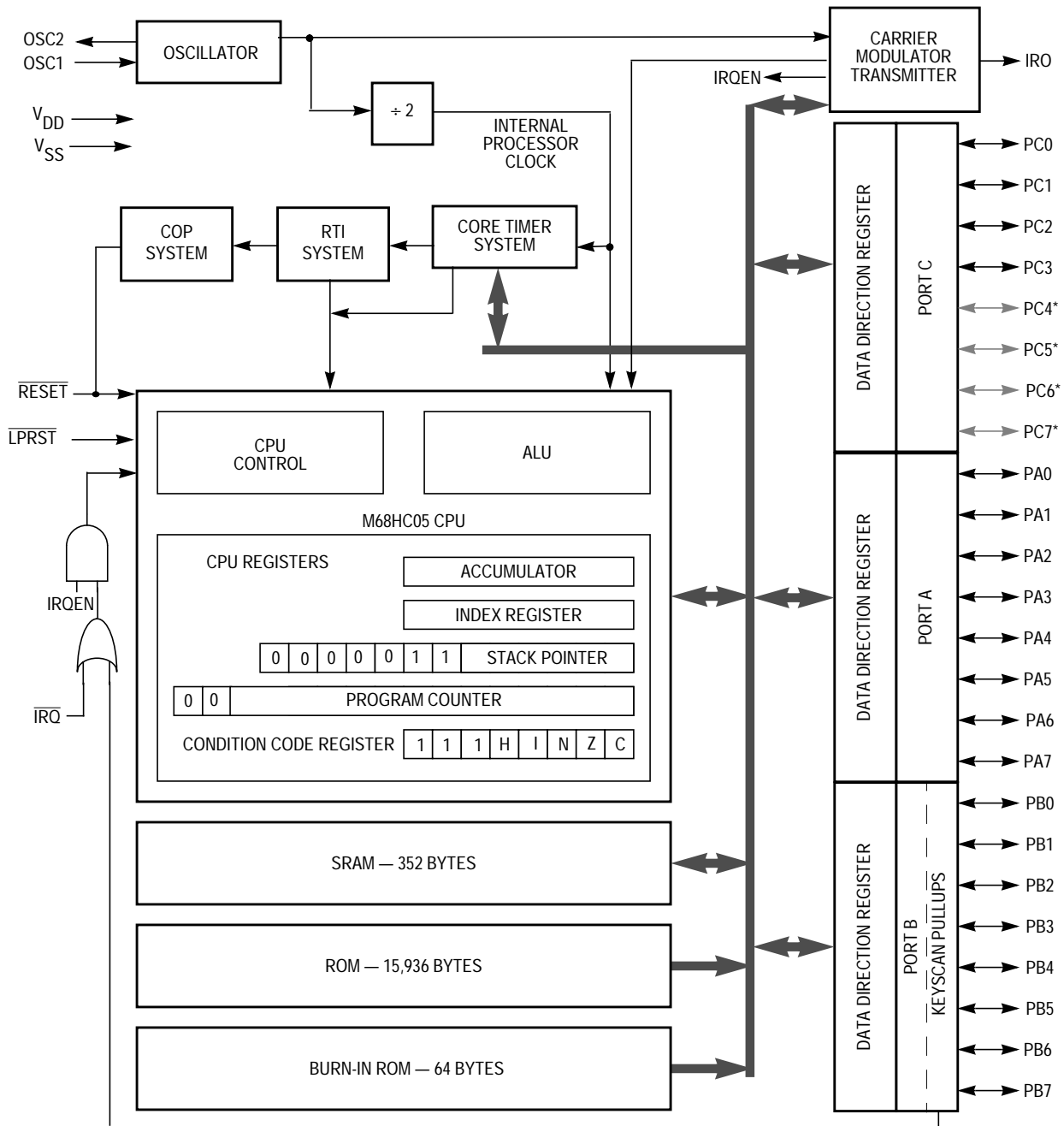
- Low Cost
- HC05 Core
- 28-Pin SOIC, 28-Pin DIP, or 44-Pin PLCC Packages
- On-Chip Oscillator with Crystal/Ceramic Resonator
- 4.2-MHz Maximum Oscillator Frequency at 2.2 to 5.0 Volt Supply
- Fully Static Operation
- 15,936 Bytes of User ROM
- 64 Bytes of Burn-In ROM
- 352 Bytes of On-Chip RAM
- 14-Stage Core Timer with Real-Time Interrupt (RTI) and Computer Operating Properly (COP) Watchdog Circuits
- Carrier Modulator Transmitter (CMT) Supporting Baseband, Pulse Length Modulator (PLM), and Frequency Shift Keying (FSK) Protocols



- Low-Power Reset Pin
- 20 Bidirectional Input/Output (I/O) Lines (Four Additional I/O Lines Available for Bond Out in Higher Pin Count Packages)
- Mask Programmable Interrupts and Pullups on Eight Port Pins (PB0–PB7)
- High-Current Infrared (IR) Drive Pin
- High-Current Port Pins (PC0–PC3)
- Power-Saving Stop and Wait Modes
- Mask Selectable Options:
  - COP Watchdog Timer
  - STOP Instruction Disable
  - Edge-Sensitive or Edge- and Level-Sensitive Interrupt Trigger
  - Port B Interrupts for Keyscan, with Two Optional Pullup Strengths

**NOTE:** *A line over a signal name indicates an active-low signal. For example,  $\overline{RESET}$  is active low.*

# General Description



\* Marked pins are available only in higher pin count (>28) packages.

**Figure 1-1. MC68HC05RC18 Block Diagram**

## 1.4 Mask Options

The MC68HC05RC18 has a total of 13 mask options, including:

- Eight Port B Interrupt Enables (one for each pin)
- Port B Pullup Enable
- Port B  $\overline{\text{Strong/Weak}}$  Pullup Select
- IRQ Sensitivity
- COP Enable/Disable
- STOP Enable/Disable

The following are nonprogrammable options in that they are selected at the time of code submission when masks are made:

### PB7IE — Port B7 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 7.

- 1 = Enables the interrupt
- 0 = Disables the interrupt

### PB6IE — Port B6 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 6.

- 1 = Enables the interrupt
- 0 = Disables the interrupt

### PB5IE — Port B5 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 5.

- 1 = Enables the interrupt
- 0 = Disables the interrupt

### PB4IE — Port B4 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 4.

- 1 = Enables the interrupt
- 0 = Disables the interrupt

### PB3IE — Port B3 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 3.

- 1 = Enables the interrupt
- 0 = Disables the interrupt

### PB2IE — Port B2 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 2.

1 = Enables the interrupt

0 = Disables the interrupt

### PB1IE — Port B1 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 1.

1 = Enables the interrupt

0 = Disables the interrupt

### PB0IE — Port B0 Interrupt Enable

This option enables or disables the interrupt generation on port B bit 0.

1 = Enables the interrupt

0 = Disables the interrupt

### PULLEN — Pullup Enable

This option will disable all pullups or enable the pullups of any port B pin that has its interrupt enabled.

1 = Enables pullups for enabled interrupts, others disabled.

0 = Disables all pullups

### SWPUSEL — $\overline{\text{Strong/Weak}}$ Pullup Select

This option selects between either the strong pullup or the weak pullup for any of the port B pullups that are enabled.

1 = Selects the weak pullups

0 = Selects the strong pullups

### COPEN — COP Enable

When the COP option is selected (COPEN = 1), the COP watchdog timer is enabled.

When the COP option is deselected (COPEN = 0), the COP watchdog timer is disabled.

### STOPEN — STOP Instruction Enable

When the STOP option is selected (STOPEN = 1), the STOP instruction is enabled.

When the STOP option is deselected (STOPEN = 0), the STOP instruction is disabled.

**NOTE:** When the STOP instruction is disabled, executing a STOP instruction is equivalent to executing a WAIT instruction, except that the core timer is reset.

**IRQ — IRQ sensitivity**

When the IRQ option is selected (LEVEL = 1), edge- and level-sensitive IRQ is enabled.

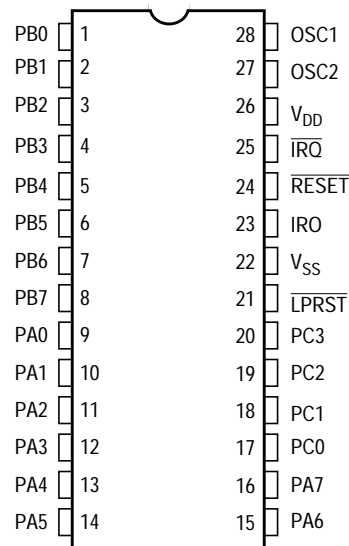
When the IRQ option is deselected (LEVEL = 0), edge-only sensitive IRQ is enabled.

## 1.5 Signal Description

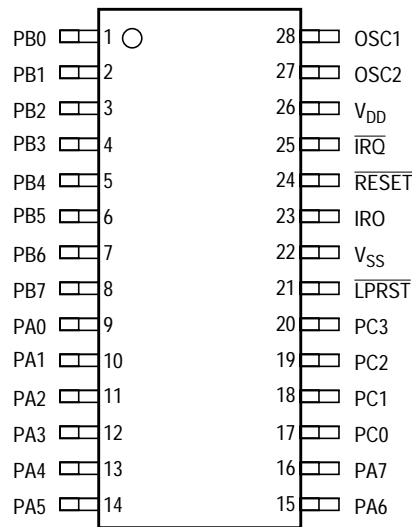
The MC68HC05RC18 is available in

1. 28-pin dual-in-line package (DIP) see [Figure 1-2](#)
2. 28-pin small outline integrated circuit (SOIC) package see [Figure 1-3](#)
3. 44-pin plastic leaded chip carrier (PLCC) package see [Figure 1-4](#)

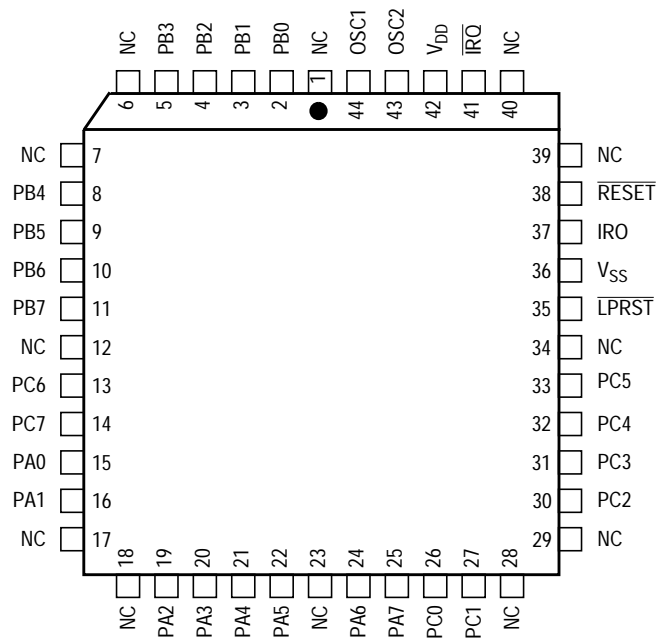
The signals are described in the following subsections.



**Figure 1-2. 28-Pin DIP Pinout**



**Figure 1-3. 28-Pin SOIC Pinout**



NOTE: NC = No Connect  
 All no connects should be tied to an appropriate logic level (either V<sub>DD</sub> or V<sub>SS</sub>).

**Figure 1-4. 44-Pin PLCC Pinout**

### 1.5.1 $V_{DD}$ and $V_{SS}$

Power is supplied to the microcontroller's digital circuits using these two pins.  $V_{DD}$  is the positive supply and  $V_{SS}$  is ground.

### 1.5.2 $\overline{IRQ}$ (Maskable Interrupt Request)

This pin has a user-specified mask option that provides one of two different choices of interrupt triggering sensitivity. The options are:

1. Negative edge-sensitive triggering only
2. Both negative edge-sensitive and level-sensitive triggering

The MCU completes the current instruction before it responds to the interrupt request. When  $\overline{IRQ}$  goes low for at least one  $t_{ILIH}$ , a logic 1 is latched internally to signify that an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic 1 and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

If the option is selected to include level-sensitive triggering, the  $\overline{IRQ}$  input requires an external resistor to  $V_{DD}$  for wired-OR operation.

The  $\overline{IRQ}$  pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

Refer to [Section 4. Interrupts](#) for more detail.

### 1.5.3 OSC1 and OSC2

The OSC1 and OSC2 pins are the control connections for the 2-pin on-chip oscillator. The oscillator can be driven by any of the following:

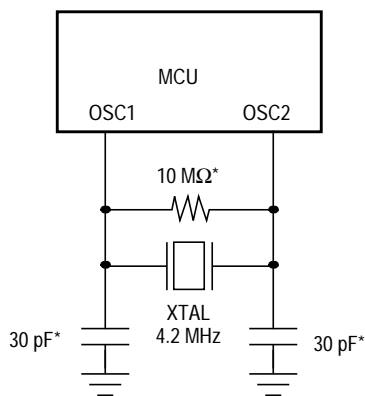
- Crystal resonator
- Ceramic resonator
- External clock signal

## General Description

**NOTE:** The frequency of the internal oscillator is  $f_{osc}$ . The MCU divides the internal oscillator by two to produce the internal clock with a frequency of  $f_{op}$ .

### 1.5.3.1 Crystal Resonator

The circuit in **Figure 1-5** shows a crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, because the crystal parameters determine the external component values required to provide reliable startup and maximum stability. The load capacitance values used in the oscillator circuit design should account for all stray layout capacitances. To minimize output distortion, mount the crystal and capacitors as close as possible to the pins.



\* Starting value only. Follow crystal supplier's recommendations regarding component values that will provide reliable startup and maximum stability.

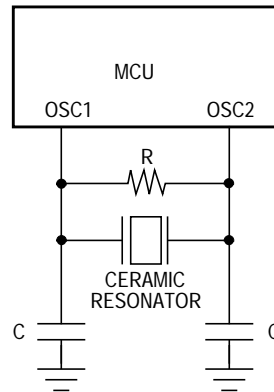
**Figure 1-5. Crystal Connections**

**NOTE:** Use an AT-cut crystal and not a strip or tuning fork crystal. The MCU might overdrive or have the incorrect characteristic impedance for a strip or tuning fork crystal.

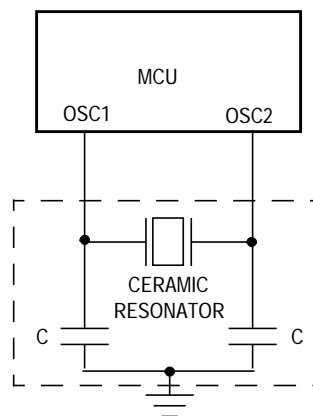


### 1.5.3.2 Ceramic Resonator

To reduce cost, use a ceramic resonator instead of a crystal. Use the circuit shown in **Figure 1-6** for a 2-pin ceramic resonator or the circuit shown in **Figure 1-7** for a 3-pin ceramic resonator and follow the resonator manufacturer's recommendations.



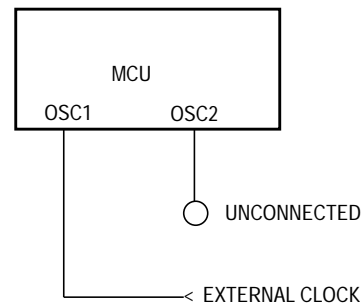
**Figure 1-6. 2-Pin Ceramic Resonator Connections**



**Figure 1-7. 3-Pin Ceramic Resonator Connections**

### 1.5.3.3 External Clock Signal

The external component values required for maximum stability and reliable starting depend upon the resonator parameters. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. To minimize output distortion, mount the resonator and capacitors as close as possible to the pins. (See [Figure 1-8](#).)



**Figure 1-8. External Clock Source Connections**

### 1.5.4 $\overline{\text{RESET}}$

This active-low pin is used to reset the MCU to a known startup state by pulling  $\overline{\text{RESET}}$  low. The  $\overline{\text{RESET}}$  pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See [Section 5. Resets](#).

### 1.5.5 $\overline{\text{LPRST}}$

The  $\overline{\text{LPRST}}$  pin is an active-low pin and is used to put the MCU into low-power reset mode. In low-power reset mode, the MCU is held in reset with all processor clocks and crystal oscillator halted. The  $\overline{\text{LPRST}}$  pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See [Section 5. Resets](#).

### 1.5.6 IRO

The IRO pin is the high-current source and sink output of the carrier modulator transmitter subsystem which is suitable for driving IR LED biasing logic. See [Section 9. Carrier Modulator Transmitter \(CMT\)](#).

### 1.5.7 PA0–PA7

These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as inputs during power-on or reset. For detailed information on I/O programming, see [6.6 Input/Output Programming](#).

### 1.5.8 PB0–PB7

These eight I/O lines comprise port B. The state of any pin is software programmable and all port B lines are configured as inputs during power-on or reset. Each port B I/O line has a mask optionable interrupt/pullup for keyscan. For detailed information on I/O programming, see [6.6 Input/Output Programming](#).

### 1.5.9 PC0–PC3 (PC4–PC7)

These eight I/O lines comprise port C. PC0–PC3 are high-current pins. PC4–PC7 are standard drive pins and are available only in higher pin count (>28) packages. The state of any pin is software programmable and all port C lines are configured as input during power-on or reset. For detailed information on I/O programming, see [6.6 Input/Output Programming](#).

**NOTE:** *Only four bits of port C are bonded out in 28-pin packages for the MC68HC05RC18, although port C is truly an 8-bit port. Since pins PC4–PC7 are unbonded, software should include the code to set their respective data direction register locations to outputs to avoid floating inputs.*

**NOTE:** *Any unused inputs and I/O ports should be tied to an appropriate logic level (either  $V_{DD}$  or  $V_{SS}$ ). Although the I/O ports of the MC68HC05RC18 do not require termination, termination is recommended to reduce the possibility of static damage.*



## Section 2. Memory

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### 2.2 Introduction

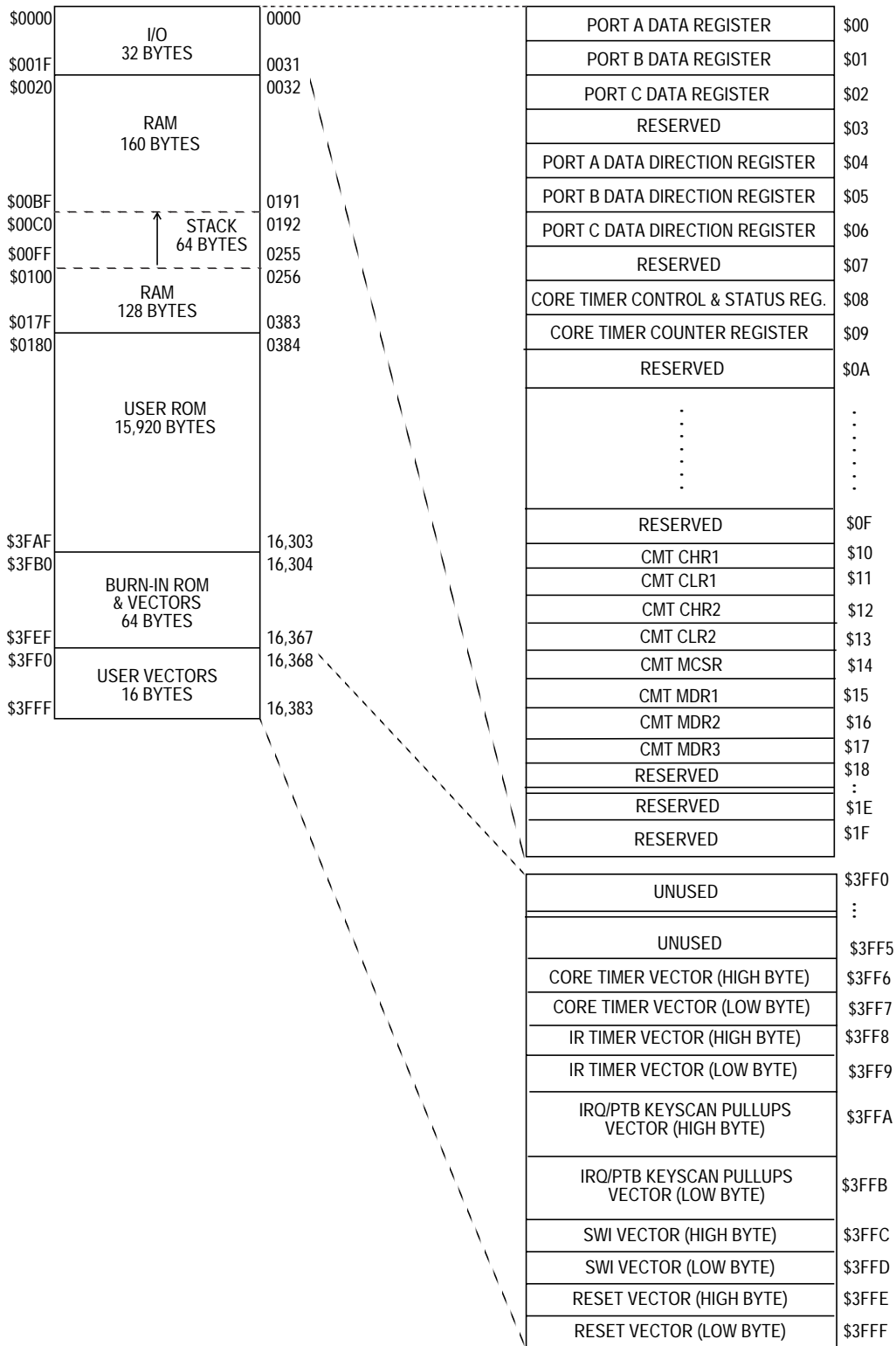
This section describes the organization of the on-chip memory.

### 2.3 Memory Map

The MC68HC05RC18 has a 16-Kbyte memory map consisting of user ROM, RAM, burn-in ROM, control registers, and input/output (I/O).

**Figure 2-1** is a memory map of the MCU. **Figure 2-2** is a more detailed memory map of the I/O register section.

# Memory



**Figure 2-1. MC68HC05RC18 Memory Map**

Addr	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$00	Port A Data Register	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
\$01	Port B Data Register	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
\$02	Port C Data Register	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
\$03	Reserved	R	R	R	R	R	R	R	R
\$04	Port A Data Direction Register	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
\$05	Port B Data Direction Register	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
\$06	Port C Data Direction Register	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
\$07	Reserved	R	R	R	R	R	R	R	R
\$08	Timer Control and Status Register	CTOF	RTIF	TOFE	RTIE	TOFC	RTFC	RT1	RT0
\$09	Timer Counter Register								
\$0A	Reserved	R	R	R	R	R	R	R	R
\$0B	Reserved	R	R	R	R	R	R	R	R
\$0C	Reserved	R	R	R	R	R	R	R	R
\$0D	Reserved	R	R	R	R	R	R	R	R
\$0E	Reserved	R	R	R	R	R	R	R	R
\$0F	Reserved	R	R	R	R	R	R	R	R
\$10	Carrier Generator High Data Register 1 (CHR1)	IROLN	CMPOL	PH5	PH4	PH3	PH2	PH1	PH0
\$11	Carrier Generator Low Data Register 1 (CLR1)	IROLP	0	PL5	PL4	PL3	PL2	PL1	PL0
\$12	Carrier Generator High Data Register 2 (CHR2)	0	0	SH5	SH4	SH3	SH2	SH1	SH0
\$13	Carrier Generator Low Data Register 2 (CLR2)	0	0	SL5	SL4	SL3	SL2	SL1	SL0
\$14	Modulator Control and Status Register (MCSR)	EOC	0	EIMSK	EXMRK	BASE	MODE	EOCIE	MCGEN
\$15	Modulator Data Register 1 (MDR1)	MB11	MB10	MB9	MB8	SB11	SB10	SB9	SB8
\$16	Modulator Data Register 2 (MDR2)	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

R = Reserved

**Figure 2-2. I/O Registers**

Addr	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$17	Modulator Data Register 3 (MDR3)	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0
\$18	Reserved	R	R	R	R	R	R	R	R
\$19	Reserved	R	R	R	R	R	R	R	R
\$1A	Reserved	R	R	R	R	R	R	R	R
\$1B	Reserved	R	R	R	R	R	R	R	R
\$1C	Reserved	R	R	R	R	R	R	R	R
\$1D	Reserved	R	R	R	R	R	R	R	R
\$1E	Reserved	R	R	R	R	R	R	R	R

R

 = Reserved

**Figure 2-2. I/O Registers (Continued)**

## 2.3.1 ROM

The user ROM consists of 15,920 bytes of ROM located from \$0180 to \$3FAF and 16 bytes of user vectors located from \$3FF0 to \$3FFF.

The burn-in ROM is located from \$3FB0 to \$3FEF.

Ten of the user vectors, \$3FF6 through \$3FFF, are dedicated to reset and interrupt vectors. The six remaining locations — \$3FF0, \$3FF1, \$3FF2, \$3FF3, \$3FF4, and \$3FF5 — are general-purpose user ROM locations.

## 2.3.2 ROM Security

Security has been incorporated into the MC68HC05RC18 to help prevent external viewing of the ROM contents. By having unique data values at locations \$2000–\$2008, customers can help ensure that their software remains proprietary.<sup>1</sup>

<sup>1</sup> No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the ROM difficult for unauthorized users.



### 2.3.3 RAM

The user RAM consists of 352 bytes of a shared stack area. The RAM starts at address \$0020 and ends at address \$017F. The stack begins at address \$00FF. The stack pointer can access 64 bytes of RAM in the range \$00FF to \$00C0.

**NOTE:** *Using the stack area for data storage or temporary work locations requires care to prevent the area from being overwritten due to stacking from an interrupt or subroutine call.*



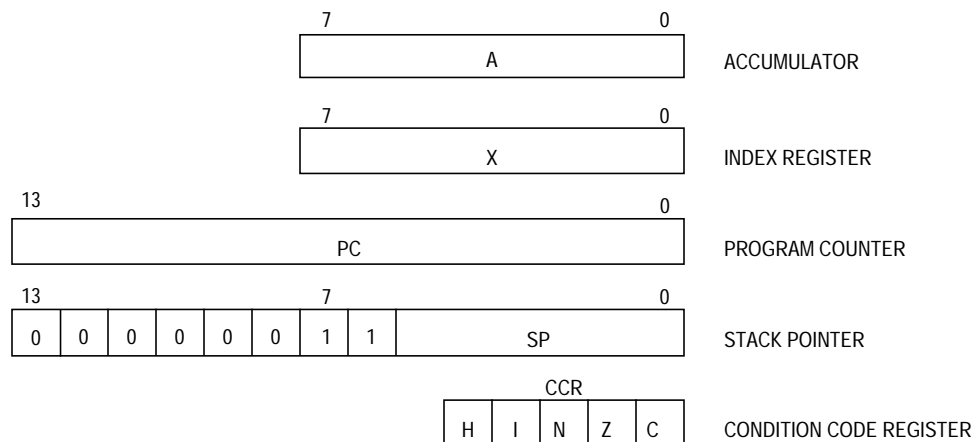
## Section 3. Central Processing Unit

### 3.1 Contents

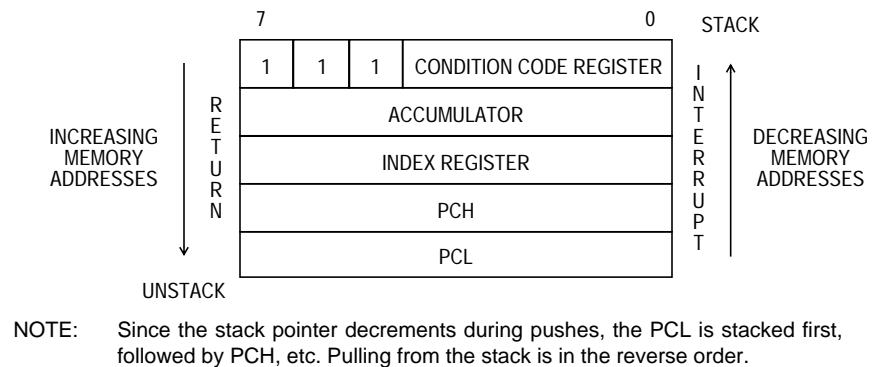
3.2	Introduction . . . . .	35
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3.5	Condition Code Register (CCR) . . . . .	36
3.6	Stack Pointer (SP) . . . . .	38
3.7	Program Counter (PC) . . . . .	38

### 3.2 Introduction

This section describes the registers of the MC68HC05RC18 central processor unit (CPU). The MCU contains five registers as shown in **Figure 3-1**. The interrupt stacking order is shown in **Figure 3-2**.



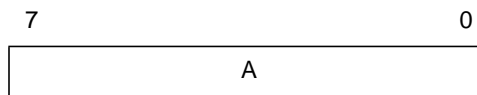
**Figure 3-1. Programming Model**



**Figure 3-2. Stacking Order**

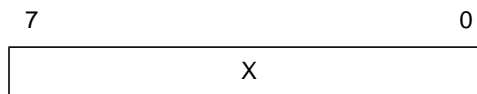
### 3.3 Accumulator (A)

The accumulator is a general-purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



### 3.4 Index Register (X)

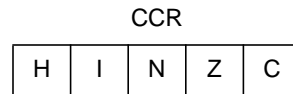
The index register is an 8-bit register used for the indexed addressing value to create an effective address. The index register may also be used as a temporary storage area.



### 3.5 Condition Code Register (CCR)

The CCR is a 5-bit register in which the H, N, Z, and C bits are used to indicate the results of the instruction just executed, and the I bit is used to enable or disable interrupts. These bits can be individually tested by

a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.



#### Half Carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

#### Interrupt (I)

When this bit is set, the timer and external interrupt are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and processed as soon as the I bit is cleared.

#### Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

#### Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

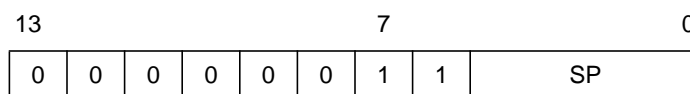
#### Carry/Borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

## 3.6 Stack Pointer (SP)

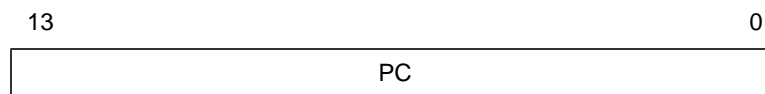
The stack pointer contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location \$00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the eight most significant bits are permanently set to 00000011. These eight bits are appended to the six least significant register bits to produce an address within the range of \$00FF to \$00C0. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and loses the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.



## 3.7 Program Counter (PC)

The program counter is a 13-bit register that contains the address of the next byte to be fetched.



**NOTE:** *The HC05 CPU core is capable of addressing 16-bit locations. For this implementation, however, the addressing registers are limited to a 16-Kbyte memory map.*

## Section 4. Interrupts

### 4.1 Contents

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4.6.3	Carrier Modulator Transmitter Interrupt (CMT) . . . . .	45
4.7	Core Timer Interrupt . . . . .	45

### 4.2 Introduction

The MCU can be interrupted four different ways, which are discussed in this section. They are:

1. Nonmaskable Software Interrupt Instruction (SWI)
2. External Asynchronous Interrupt ( $\overline{\text{IRQ}}$ /Port B Keyscan)
3. Internal Carrier Modulator Transmitter Interrupt
4. Internal Core Timer Interrupt

## 4.3 CPU Interrupt Processing

Interrupts cause the processor to save register contents on the stack and to set the interrupt mask (I bit) to prevent additional interrupts. Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete.

If interrupts are not masked (I bit in the CCR is clear) when the CPU receives an interrupt request, the processor will proceed with interrupt processing. Otherwise, the next instruction is fetched and executed. If an interrupt occurs, the processor completes the current instruction, stacks the current CPU register state, sets the I bit to inhibit further interrupts, and finally checks the pending hardware interrupts. If more than one interrupt is pending after the stacking operation, the interrupt with the highest vector location shown in [Table 4-1](#) will be serviced first. The SWI is executed the same as any other instruction, regardless of the I-bit state.

When an interrupt is to be processed, the CPU fetches the address of the appropriate interrupt software service routine from the vector table at locations \$3FF6–\$3FFF as defined in [Table 4-1](#).

The M68HC05 CPU does not support interruptible instructions. The maximum latency to the first instruction of the interrupt service routine must include the longest instruction execution time plus stacking overhead.

$$\text{Latency} = (\text{Longest instruction execution time} + 10) \times t_{\text{cyc}} \text{ seconds}$$

An RTI instruction is used to signify when the interrupt software service routine is completed. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume at the next instruction that was to be executed when the interrupt took place. [Figure 4-1](#) shows the sequence of events that occurs during interrupt processing.



## 4.4 Reset Interrupt Sequence

The reset function is not in the strictest sense an interrupt; however, it is acted upon in a similar manner as shown in [Figure 4-1](#). A low-level input on the  $\overline{\text{RESET}}$  pin or an internally generated RST signal, causes the program to vector to its starting address, which is specified by the contents of memory locations \$3FFE and \$3FFF. The I bit in the condition code register is also set. The MCU is configured to a known state during this type of reset.

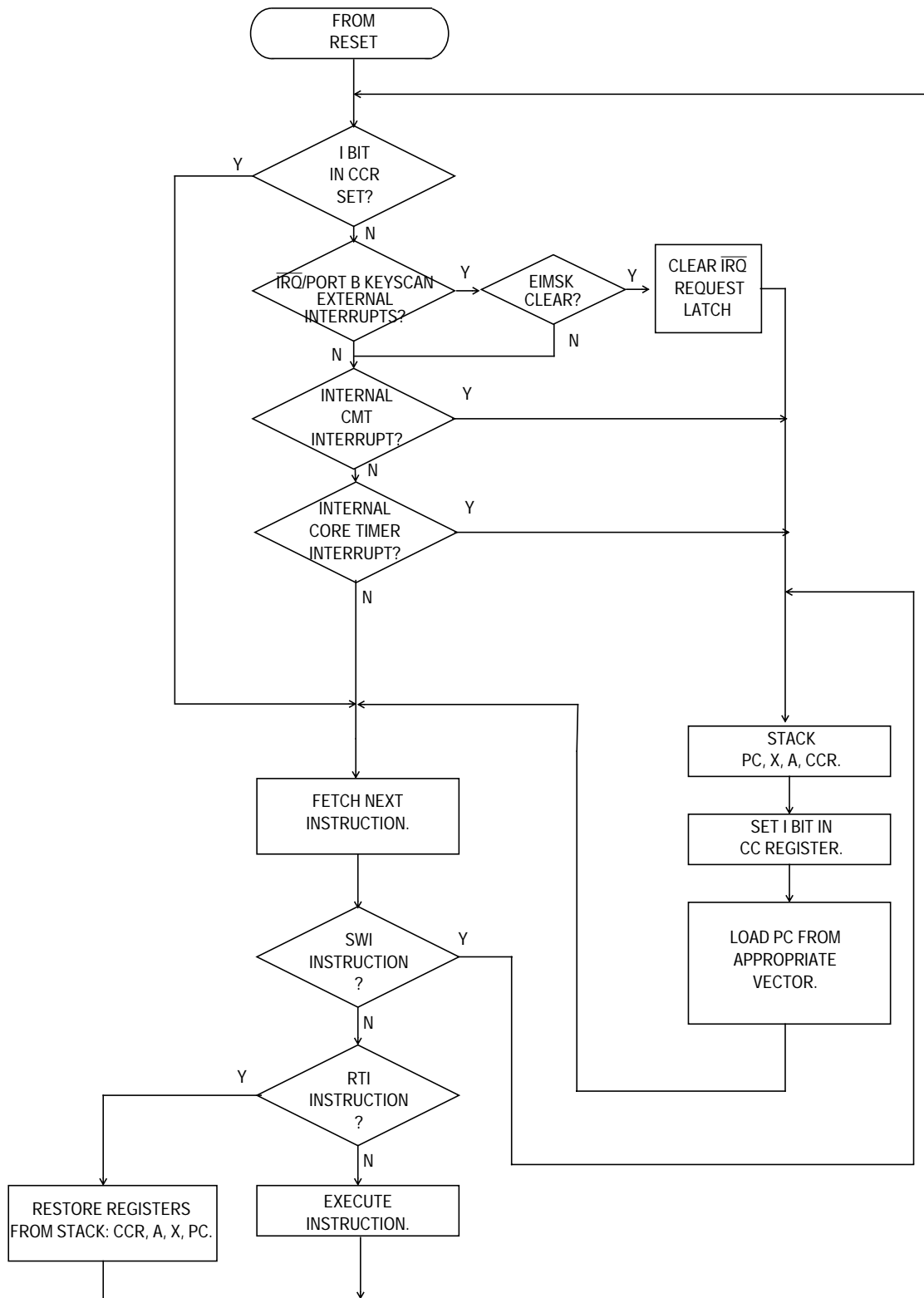
**Table 4-1. Vector Address for Interrupts and Reset**

Register	Flag Name	Interrupt	CPU Interrupt	Vector Address
N/A	N/A	Reset	RESET	\$3FFE–\$3FFF
N/A	N/A	Software Interrupt	SWI	\$3FFC–\$3FFD
N/A	N/A	External Interrupts*	IRQ	\$3FFA–\$3FFB
MCSR	EOC	End of Cycle Interrupt	CMT	\$3FF8–\$3FF9
CTCSR	CTOF, RTIF	Real Time Interrupt Core Timer Overflow	CORE TIMER	\$3FF6–\$3FF7

\*External interrupts include  $\overline{\text{IRQ}}$  and port B keyscan sources.

## 4.5 Software Interrupt (SWI)

The SWI is an executable instruction and a nonmaskable interrupt since it is executed regardless of the state of the I bit in the CCR. If the I bit is zero (interrupts enabled), the SWI instruction executes after interrupts that were pending before the SWI was fetched or before interrupts generated after the SWI was fetched. The interrupt service routine address is specified by the contents of memory locations \$3FFC and \$3FFD.



**Figure 4-1. Interrupt Processing Flowchart**

## 4.6 Hardware Interrupts

All hardware interrupts except RESET are maskable by the I bit in the CCR. If the I bit is set, all hardware interrupts (internal and external) are disabled. Clearing the I bit enables the hardware interrupts.

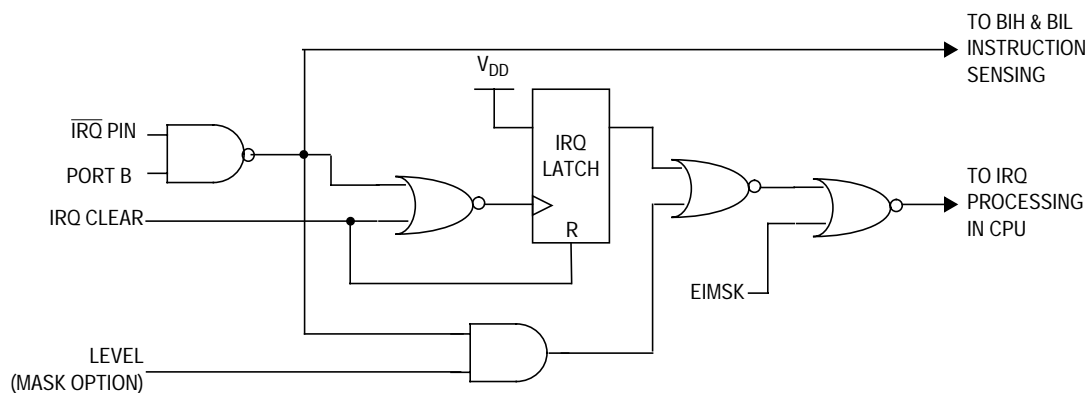
The three types of hardware interrupts, which are explained in the following sections, are:

1. External interrupt
2. Core timer interrupt
3. Carrier modulator transmitter interrupt

### 4.6.1 External Interrupt (IRQ/Port B Keyscan)

The  $\overline{\text{IRQ}}$  pin provides an asynchronous interrupt to the CPU. A block diagram of the IRQ function is shown in [Figure 4-2](#).

**NOTE:** *The BIH and BIL instructions will apply to the level on the  $\overline{\text{IRQ}}$  pin itself and to the output of the logic OR function with the port B IRQ interrupts. The states of the individual port B pins can be checked by reading the appropriate port B pins as inputs.*



**Figure 4-2. IRQ Function Block Diagram**

The  $\overline{\text{IRQ}}$  pin is one source of an external interrupt. All port B pins (PB0–PB7) act as other external interrupt sources if their interrupt feature is enabled as specified by the user.

When edge sensitivity is selected for the IRQ interrupt, it is sensitive to two cases:

1. Falling edge on the  $\overline{\text{IRQ}}$  pin
2. Falling edge on any port B pin with interrupt enabled

When edge and level sensitivity is selected for the IRQ interrupt, it is sensitive to three cases:

1. Low level on the  $\overline{\text{IRQ}}$  pin
2. Falling edge on the  $\overline{\text{IRQ}}$  pin
3. Falling edge or low level on any port B pin with interrupt enabled

External interrupts can also be masked by setting the EIMSK bit in the MSCR register of the IR remote timer. See [9.5.4 Modulator Period Data Registers \(MDR1, MDR2, and MDR3\)](#) for details. When masked, any external interrupt received sets the interrupt latch and remains pending within the interrupt module until the EIMSK bit is cleared, at that point, the external interrupt will be forwarded to the CPU for processing. Reset clears the interrupt latch, as will the CPU when it finishes processing the external interrupt.

## 4.6.2 External Interrupt Timing

If the interrupt mask bit (I bit) of the CCR is set, all maskable interrupts (internal and external) are disabled. Clearing the I bit enables interrupts. The interrupt request is latched immediately following the falling edge of the  $\overline{\text{IRQ}}$  source. The interrupt request is then synchronized internally and serviced as specified by the contents of \$3FFA and \$3FFB.

Either a level-sensitive and edge-sensitive trigger or an edge-sensitive-only trigger is available via the mask programmable option for the  $\overline{\text{IRQ}}$  pin.

### 4.6.3 Carrier Modulator Transmitter Interrupt (CMT)

A CMT interrupt is generated when the end of cycle flag (EOC) and the end of cycle interrupt enable (EOCIE) bits are set in the modulator control and status register (MCSR). This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations \$3FF8 and \$3FF9. Note that the CMT will not generate any new interrupts while the chip is in wait mode, regardless of the state of the status register (MCSR).

## 4.7 Core Timer Interrupt

This timer can create two types of interrupts. A timer overflow interrupt occurs whenever the 8-bit timer rolls over from \$FF to \$00 and the enable bit TOFE is set. A real-time interrupt occurs whenever the programmed time elapses and the enable bit RTIE is set. Either of these interrupts vectors to the same interrupt service routine, located at the address specified by the contents of memory locations \$3FF6 and \$3FF7.



## Section 5. Resets

### 5.1 Contents

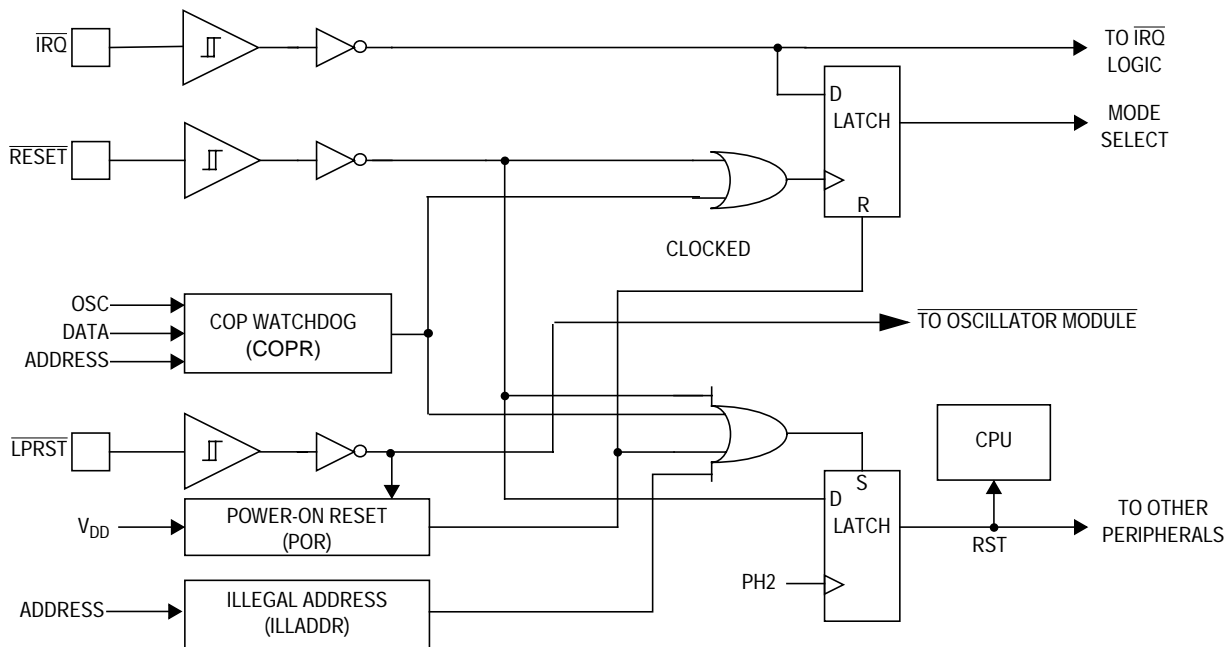
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### 5.2 Introduction

The MCU can be reset from five sources: two external inputs and three internal restart conditions. The  $\overline{\text{RESET}}$  and  $\overline{\text{LPRST}}$  pins are inputs as shown in [Figure 5-1](#). All the internal peripheral modules will be reset by the internal reset signal (RST). Refer to [Figure 5-2](#) for reset timing detail.

## 5.3 External Reset ( $\overline{\text{RESET}}$ )

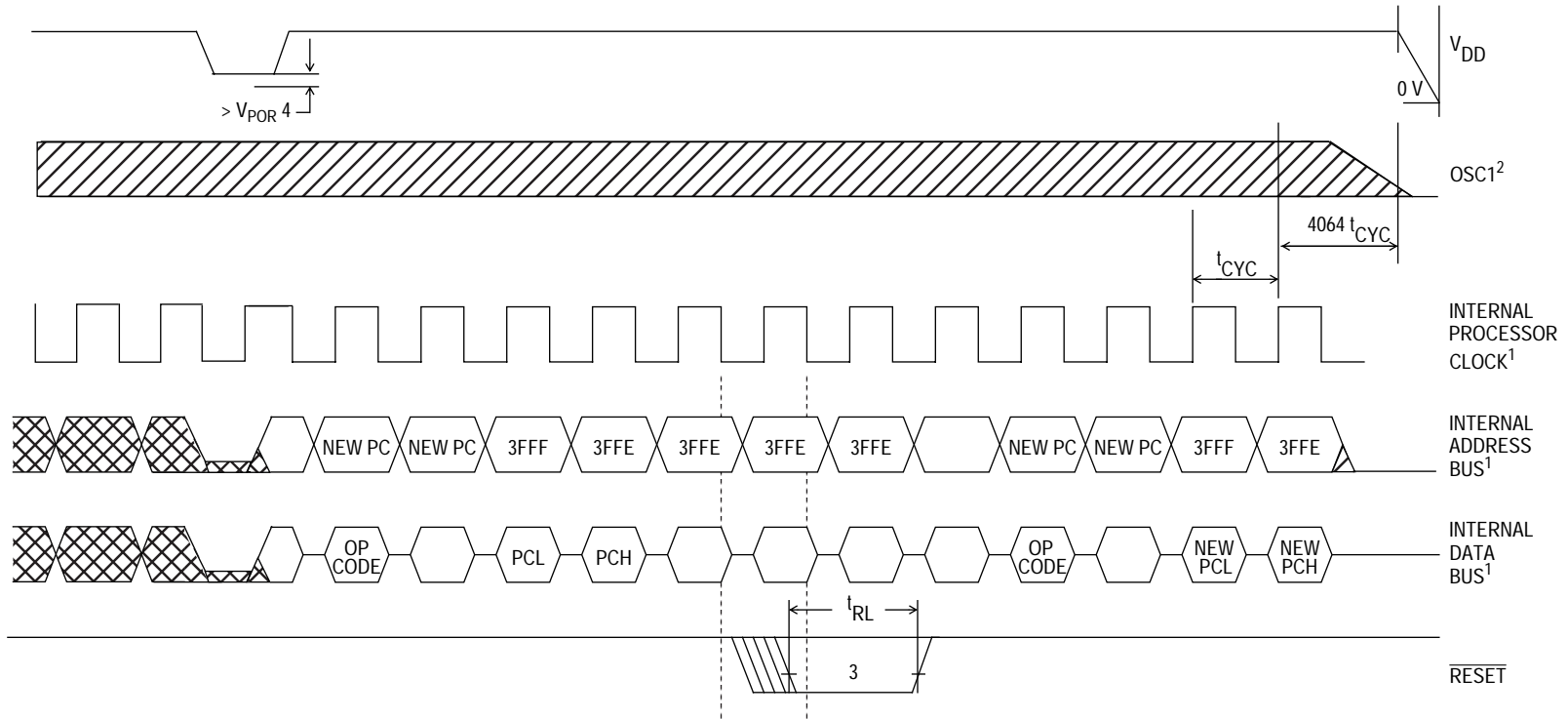
The  $\overline{\text{RESET}}$  pin is one of the two external sources of a reset. This pin is connected to a Schmitt trigger input gate to provide an upper and lower threshold voltage separated by a minimum amount of hysteresis. This external reset occurs whenever the  $\overline{\text{RESET}}$  pin is pulled below the lower threshold and remains in reset until the  $\overline{\text{RESET}}$  pin rises above the upper threshold. This active-low input will generate the RST signal and reset the CPU and peripherals. Termination of the external  $\overline{\text{RESET}}$  input or the internal COP watchdog reset are the only reset sources that can place the MCU in a nonuser operating mode. POR and  $\overline{\text{LPRST}}$  place the MCU in user mode while the illegal address reset has no effect on operating mode.



**Figure 5-1. Reset Block Diagram**

**NOTE:** Activation of the RST signal is generally referred to as reset of the device, unless otherwise specified.





NOTES:

1. Internal timing signal and bus information is not available externally.
2.  $OSC1$  line is not meant to represent frequency. It is only used to represent time.
3. The next rising edge of the internal processor clock following the rising edge of  $\overline{RESET}$  initiates the reset sequence.
4.  $V_{DD}$  must fall to a level lower than  $V_{POR}$  to be recognized as a power-on reset on the next rise of  $V_{DD}$ .

Figure 5-2. Reset and POR Timing Diagram

## 5.4 Low-Power External Reset ( $\overline{\text{LPRST}}$ )

This pin is connected to a Schmitt trigger input gate to provide an upper and lower threshold voltage separated by a minimum amount of hysteresis. The  $\overline{\text{LPRST}}$  pin is one of the two external sources of a reset. This external reset occurs whenever the  $\overline{\text{LPRST}}$  pin is pulled below the lower threshold and remains in reset until the  $\overline{\text{LPRST}}$  pin rises above the upper threshold. This active-low input will, in addition to generating the RST signal and resetting the CPU and peripherals, halt all internal processor clocks and the crystal oscillator. The MCU will remain in this low-power reset condition as long as a logic 0 remains on  $\overline{\text{LPRST}}$ . When a logic 1 is applied to  $\overline{\text{LPRST}}$ , processor clocks will be re-enabled with the MCU remaining in reset until the 4064 internal processor clock cycle ( $t_{\text{cyc}}$ ) oscillator stabilization delay is completed. If any other reset function is active at the end of this 4064-cycle delay, the RST signal remains in the reset condition until the other reset condition(s) end.

## 5.5 Internal Resets

The three internally generated resets are the initial power-on reset function, the COP watchdog timer reset, and the illegal address detector. Termination of the external  $\overline{\text{RESET}}$  input or the internal COP watchdog timer are the only reset sources that can place the MCU into a non-user operating mode. POR and  $\overline{\text{LPRST}}$  place the MCU in user mode while the illegal address reset has no effect on operating mode.

### 5.5.1 Power-On Reset (POR)

The internal POR is generated on power-up to allow the clock oscillator to stabilize. The POR is strictly for power turn-on conditions and is not able to detect a drop in the power supply voltage (brown-out). There is an oscillator stabilization delay of 4064 internal processor bus clock cycles (PH2) after the oscillator becomes active.

The POR generates the RST signal that resets the CPU. If any other reset function is active at the end of this 4064-cycle delay, the RST signal remains in the reset condition until the other reset condition(s) ends.

**CAUTION:** *The  $V_{DD}$  voltage should rise sufficiently fast to reach the minimum operating voltage for the given oscillator frequency before the 4064-cycle internal processor clock timeout period expires. If  $V_{DD}$  rises too slowly, then either the  $\overline{RESET}$  or  $\overline{LPRST}$  pin should be driven low (less than  $V_{IL}$ ) until  $V_{DD}$  reaches the minimum operating level for the oscillator frequency.*

## 5.5.2 Computer Operating Properly Reset (COPR)

The MCU contains a watchdog timer that automatically times out if not reset (cleared) within a specific time by a program reset sequence. If the COP watchdog timer is allowed to timeout, an internal reset is generated to reset the MCU.

The COP reset function is enabled or disabled by a mask option and is verified during production testing.

### 5.5.2.1 Resetting the COP

Writing a zero to the COPF bit prevents a COP reset. This action resets the counter and begins the timeout period again. The COPF bit is bit 0 of address \$3FF0. A read of address \$3FF0 returns user data programmed at that location.

### 5.5.2.2 COP During Wait Mode

The COP continues to operate normally during wait mode. The software should pull the device out of wait mode periodically and reset the COP by writing to the COPF bit to prevent a COP reset.

### 5.5.2.3 COP During Stop Mode

When STOP is executed, the COP counter will be cleared and held in that state until the STOP state is exited. This is true whether STOP is enabled and the chip enters an actual STOP state (when all clocks are stopped) or if STOP is disabled and only the internal PH1 and PH2 are stopped (a wait-like state). If a reset is used to exit stop mode, the COP counter is held in reset until 4064 POR cycles are completed, at which

time counting will begin. If an external IRQ is used to exit stop mode, the COP counter does not wait for the completion of the 4064 POR cycles but does count these cycles.

#### 5.5.2.4 COP Watchdog Timer Considerations

The COP watchdog timer is active in all modes of operation if enabled by a mask option. If the COP watchdog timer is selected by a mask option, any execution of the STOP instruction (either intentionally or inadvertently due to the CPU being disturbed) causes the oscillator to halt and prevents the COP watchdog timer from timing out. If the COP watchdog timer is selected by a mask option, the COP resets the MCU when it times out. Therefore, it is recommended that the COP watchdog be **disabled** for a system that must have intentional uses of the wait mode for periods longer than the COP timeout period.

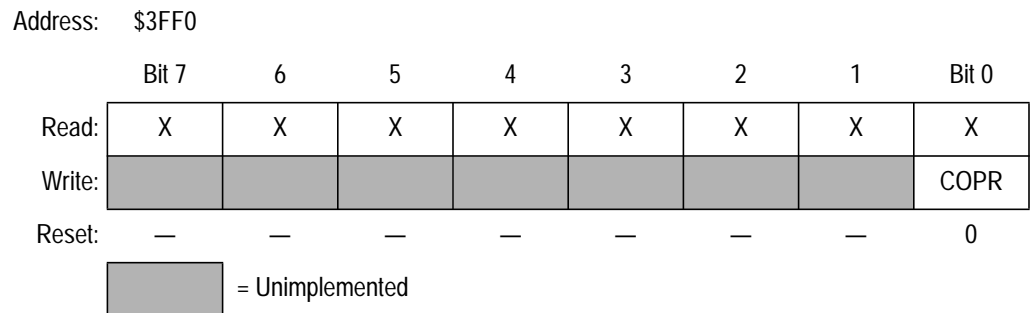
The recommended interactions and considerations for the COP watchdog timer, STOP instruction, and WAIT instruction are summarized in [Table 5-1](#).

**Table 5-1. COP Watchdog Timer Recommendations**

IF the Following Conditions Exist:	THEN the COP Watchdog Timer Should Be:
Wait Time	
Wait Time <b>Less than</b> COP Timeout	Enable or Disable COP by Mask Option
Wait Time <b>More than</b> COP Timeout	Disable COP by Mask Option
Any Length Wait Time	Disable COP by Mask Option

### 5.5.2.5 COP Register

The COP register is shared with the LSB of the unimplemented user interrupt vector at location \$3FF0 as shown in **Figure 5-3**. Reading this location returns whatever user data has been programmed at this location. Writing a 0 to the COPR bit in this location clears the COP watchdog timer.



**Figure 5-3. COP Watchdog Timer Location**

### 5.5.3 Illegal Address

An illegal address reset is generated when the CPU attempts to fetch an instruction from I/O address space (\$0000 to \$001F).



## Section 6. Parallel Input/Output (I/O)

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### 6.2 Introduction

In user mode, 24 lines (four of which are unavailable in the standard 28-pin package) are arranged as three 8-bit I/O ports. These ports are programmable as either inputs or outputs under software control of the data direction registers.

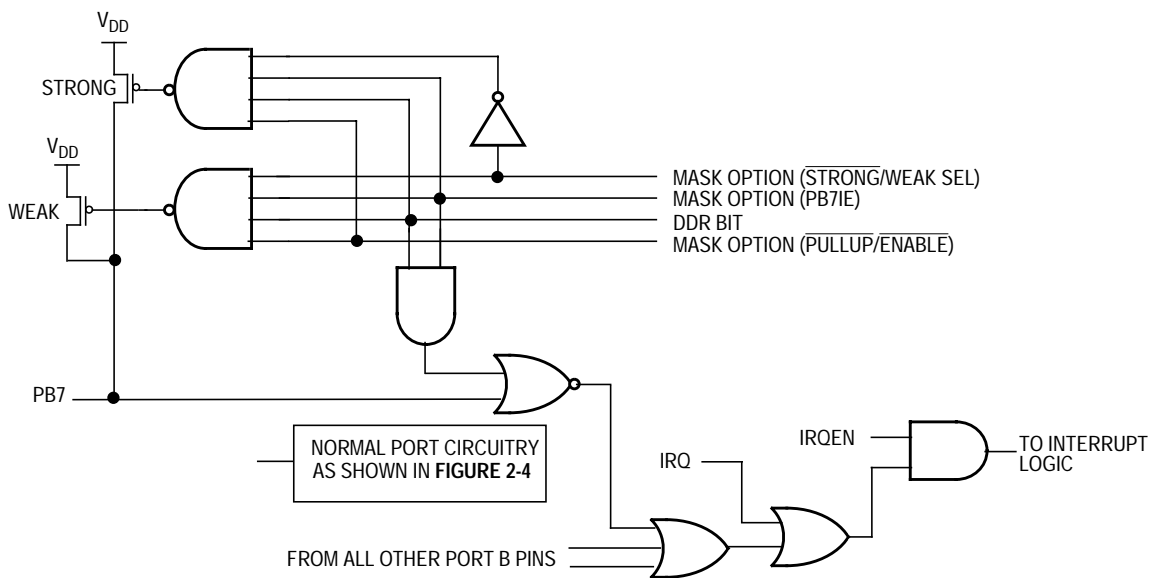
**NOTE:** *To avoid a glitch on the output pins, write data to the I/O port data register before writing a one to the corresponding data direction register.*

### 6.3 Port A

Port A is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The port A data register is at \$0000 and the data direction register (DDR) is at \$0004. Reset does not affect the data register, but clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

## 6.4 Port B

Port B is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The address of the port B data register is \$0001 and the data direction register (DDR) is at address \$0005. Reset does not affect the data register, but clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode. Each of the port B pins has a mask programmable interrupt generation option, any of which can be enabled. When an interrupt option is enabled, this pin may also have a pullup resistor enabled. There is a choice between two pullup strengths, either of which may be active for the enabled interrupts. The choice of whether to enable the pullups and which strength to choose will be the same for all enabled interrupts circuits. The edge or edge and level sensitivity of the  $\overline{IRQ}$  pin will also pertain to the enabled port B pins. Be careful when using port B pins that have the interrupt generation enabled. Before switching from an output to an input, the data should be preconditioned to a logic 1 to prevent an interrupt from being generated or the I bit of the condition code register should be set to prevent any such generated interrupt from taking immediate effect.



**Figure 6-1. Port B Pullup Options**



## 6.5 Port C

Port C is an 8-bit bidirectional port (PC0–PC7) which does not share any of its pins with other subsystems. The port C data register is at \$0002 and the data direction register (DDR) is at \$0006. Reset does not affect the data register, but clears the data direction register, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode. Port C pins PC4–PC7 are available only in higher pin count (>28 pin) packages.

**NOTE:** *Only four bits of port C are bonded out in 28-pin packages for the MC68HC05RC18, although port C is truly an 8-bit port. Since pins PC4–PC7 are unbonded, software should include the code to set their respective data direction register locations to outputs to avoid floating inputs.*

## 6.6 Input/Output Programming

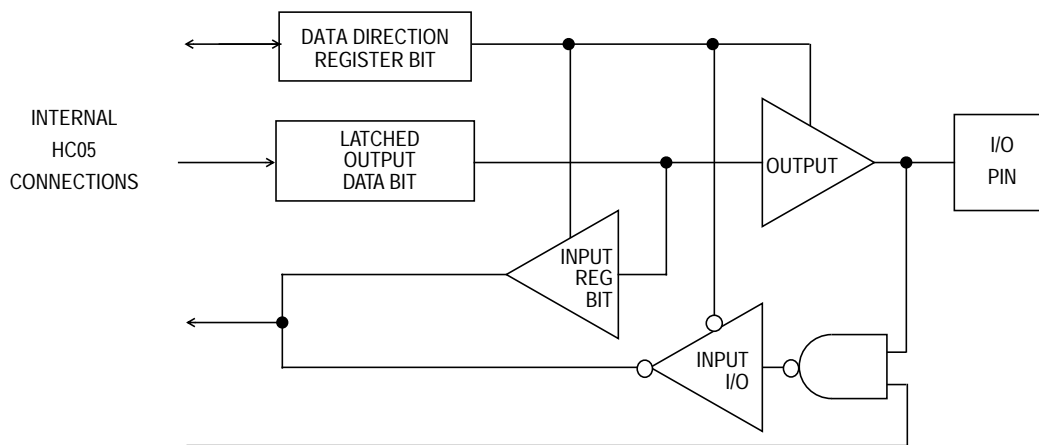
Port pins can be programmed as inputs or outputs under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each I/O port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set to a logic 1. A pin is configured as an input if its corresponding DDR bit is cleared to a logic 0.

At power-on or reset, all DDRs are cleared, which configures all pins as inputs. The data direction registers are capable of being written to or read by the processor. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin.

# Parallel Input/Output (I/O)

**Table 6-1. I/O Pin Functions**

Access	DDR	I/O Pin Functions
Write	0	The I/O pin is in input mode. Data is written into the output data latch.
Write	1	Data is written into the output data latch and output to the I/O pin.
Read	0	The state of the I/O pin is read.
Read	1	The I/O pin is in an output mode. The output data latch is read.



**Figure 6-2. I/O Circuitry**

## Section 7. Low-Power Modes

### 7.1 Contents

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7.4	Stop Recovery . . . . .	60
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7.6	Low-Power Reset . . . . .	61

### 7.2 Introduction

This section describes the low-power modes, which are stop mode and wait mode.

### 7.3 Stop Mode

The STOP instruction places the MCU in its lowest power-consumption mode. In stop mode, the internal oscillator is turned off, halting all internal processing, including timer operation.

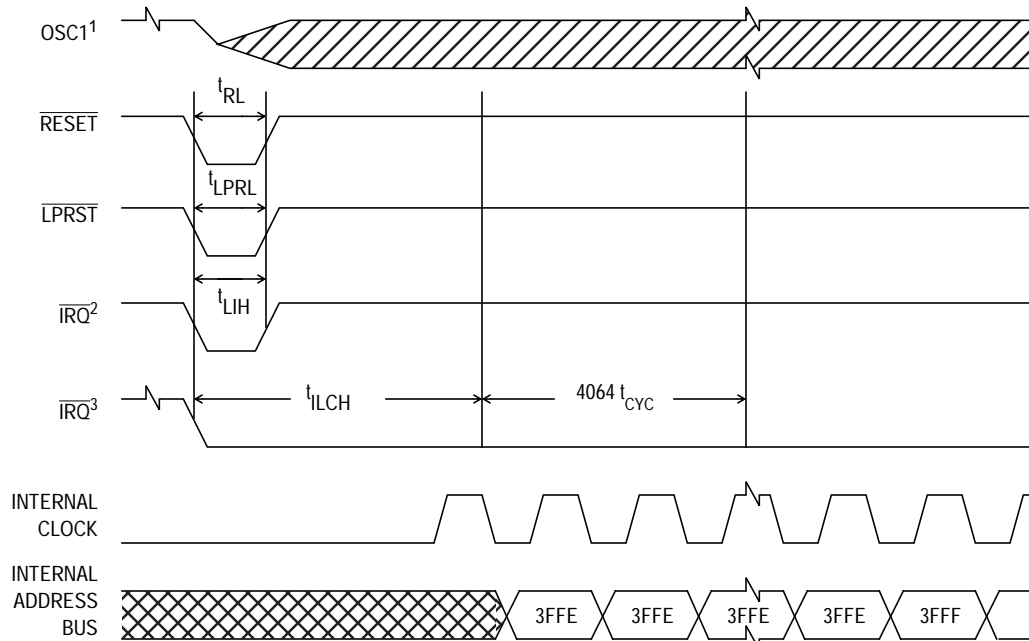
When stop mode is entered, all core timer counter bits are cleared. The I bit in the CCR is cleared to enable interrupts, but all interrupts are held pending until the device is brought out of stop mode. All other registers and memory remain unaltered. All input/output lines remain unchanged.

**NOTE:** *If an external interrupt is pending when stop mode is entered, then stop mode will be exited immediately.*

*The EIMSK bit is not cleared automatically by the execution of a STOP instruction. Care should be taken to clear this bit before entering stop mode.*

## 7.4 Stop Recovery

The processor can be brought out of stop mode only by an external interrupt,  $\overline{\text{LPRST}}$ , or  $\overline{\text{RESET}}$ . Refer to [Figure 7-1](#).



- NOTES:
1. Represents the internal gating of the OSC1 pin
  2.  $\overline{\text{IRQ}}$  pin edge-sensitive mask option
  3.  $\overline{\text{IRQ}}$  pin level- and edge-sensitive mask option

RESET OR INTERRUPT  
VECTOR FETCH

**Figure 7-1. Stop Recovery Timing Diagram**

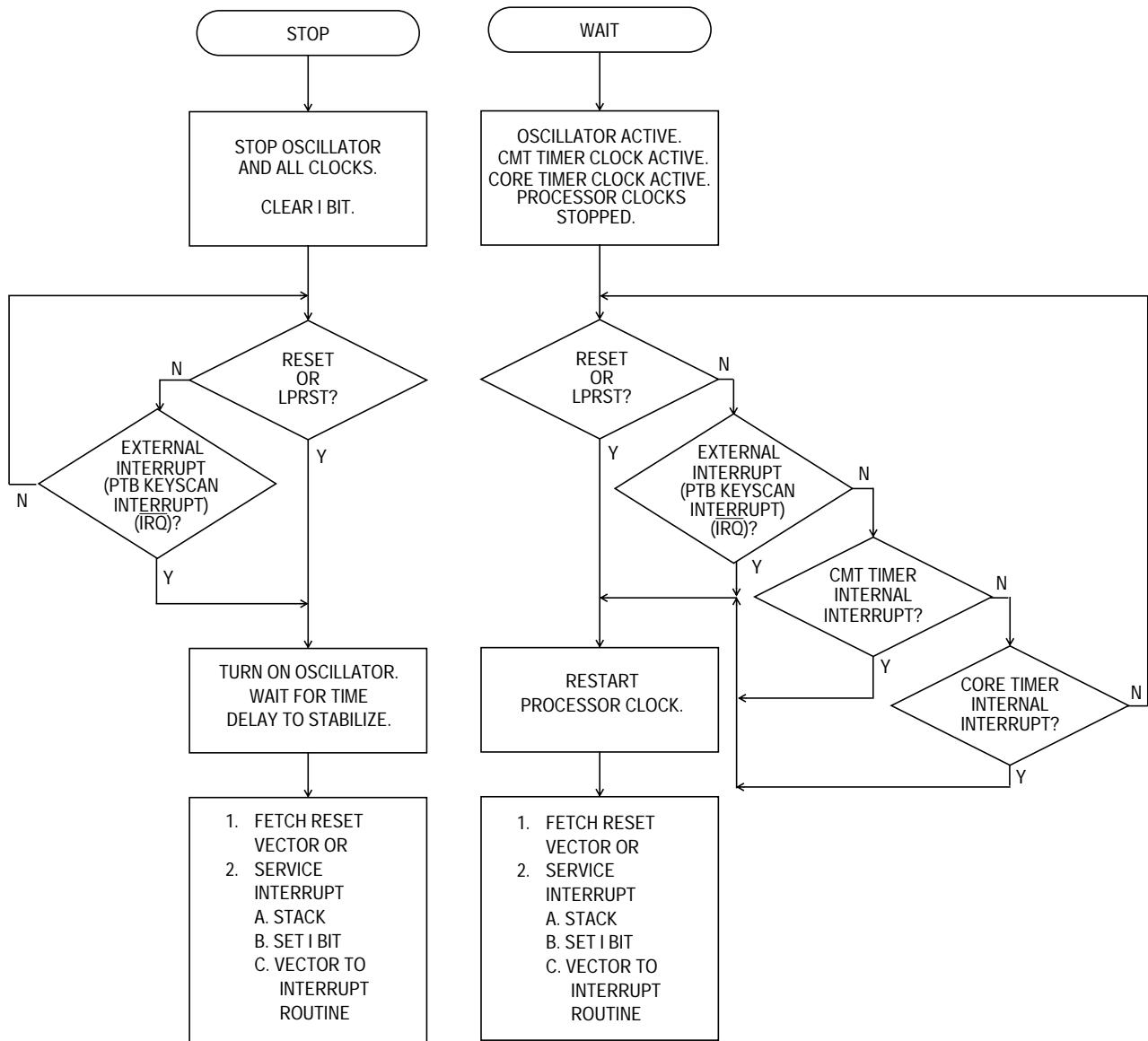
## 7.5 Wait Mode

The WAIT instruction places the MCU in a low power-consumption mode, but the wait mode consumes more power than the stop mode. All CPU action is suspended, but the core timer, the oscillator, and any enabled module remain active. Any interrupt or reset will cause the MCU to exit wait mode. The user must shut off subsystems to reduce power consumption. Wait current specifications assume CPU operation only and do not include current consumption by any other subsystems.

During wait mode, the I bit in the CCR is cleared to enable interrupts. All other registers, memory, and input/output lines remain in their previous states. The timer can be enabled to allow a periodic exit from wait mode.

## 7.6 Low-Power Reset

Low-power reset mode is entered when a logic 0 is detected on the  $\overline{\text{LPRST}}$  pin. When in this mode (as long as  $\overline{\text{LPRST}}$  is held low), the MCU is held in reset and all internal clocks and the crystal oscillator (if used) are halted. Applying a logic 1 to  $\overline{\text{LPRST}}$  will cause the part to exit low-power reset mode and begin counting out the 4064-cycle oscillator stabilization period. Once this time has elapsed, the MCU will begin operation from the reset vectors (\$3FFE–\$3FFF).



**Figure 7-2. Stop/Wait Flowchart**

## Section 8. Core Timer

### 8.1 Contents

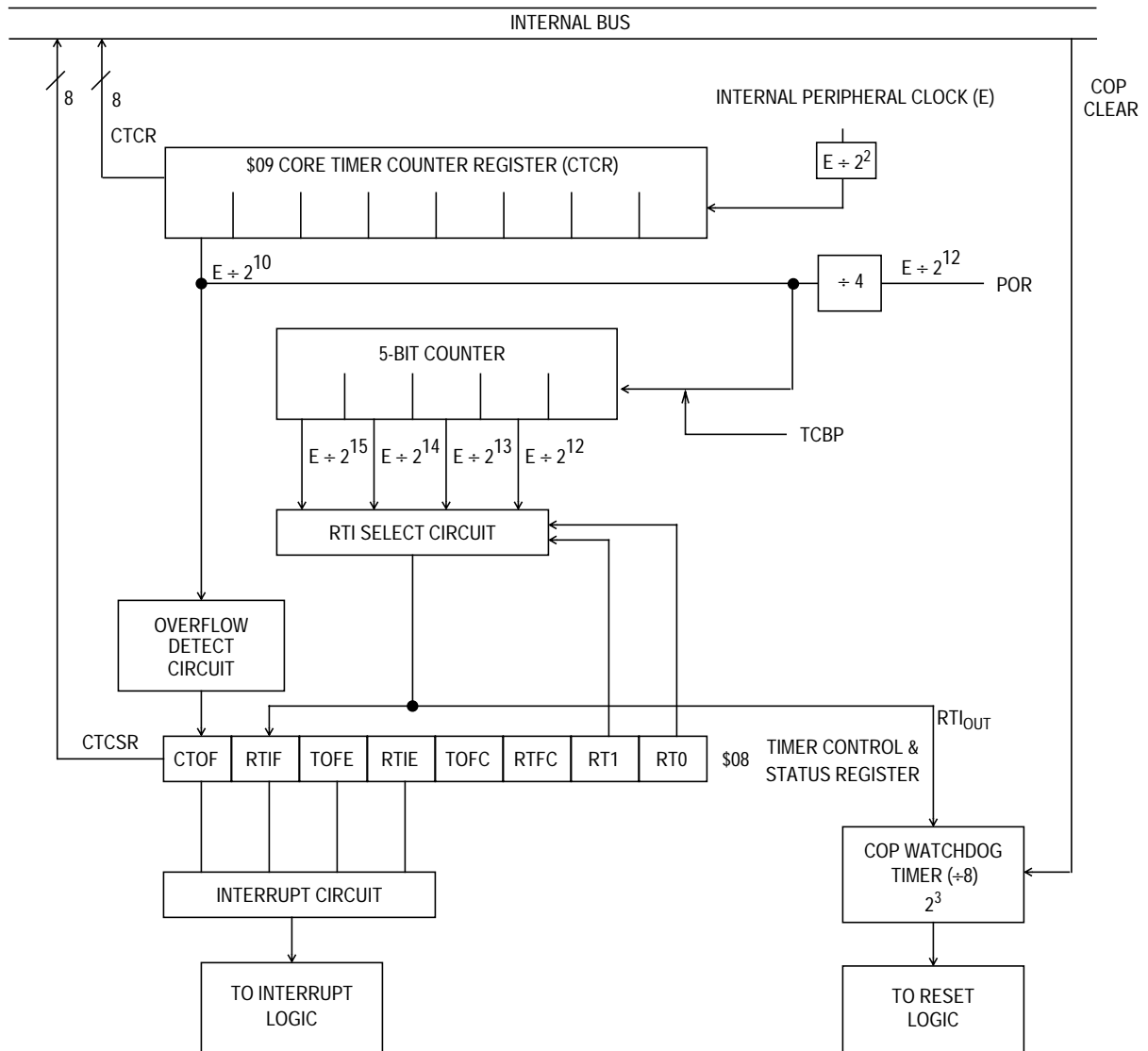
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### 8.2 Introduction

The core timer for this device is a 14-stage multifunctional ripple counter. Features include timer overflow, power-on reset (POR), real-time interrupt (RTI), and COP watchdog timer.

As seen in **Figure 8-1**, the internal peripheral clock is divided by four and then drives an 8-bit ripple counter. The value of this 8-bit ripple counter can be read by the CPU at any time by accessing the core timer counter register (CTCR) at address \$09. A timer overflow function is implemented on the last stage of this counter, giving a possible interrupt rate of the internal peripheral clock (E)/1024. This point is then followed by three more stages, with the resulting clock (E/4096) driving the real-time interrupt circuit (RTI). The RTI circuit consists of three divider stages with a one-of-four selector. The output of the RTI circuit is further divided by eight to drive the mask optional COP watchdog timer circuit. The RTI rate selector bits and the RTI and CTOF enable bits and flags are located in the timer control and status register at location \$08.

# Core Timer



**Figure 8-1. Core Timer Block Diagram**



### 8.3 Core Timer Control and Status Register

The CTCSR contains the timer interrupt flag, the timer interrupt enable bits, and the real-time interrupt rate select bits. **Figure 8-2** shows the value of each bit in the CTCSR when coming out of reset.

Address: \$0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CTOF	RTIF	TOFE	RTIE	0	0	RT1	RT0
Write:					TOFC	RTFC		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

**Figure 8-2. Core Timer Control and Status Register (CTCSR)**

#### CTOF — Core Timer Overflow

CTOF is a read-only status bit set when the 8-bit ripple counter rolls over from \$FF to \$00. Clearing the CTOF is done by writing a one to TOFC. Writing to this bit has no effect. Reset clears CTOF.

#### RTIF — Real-Time Interrupt Flag

The real-time interrupt circuit consists of a 3-stage divider and a one-of-four selector. The clock frequency that drives the RTI circuit is  $E/2^{12}$  (or  $E \div 4096$ ) with three additional divider stages giving a maximum interrupt period of 16 milliseconds at a bus rate of 2.024 MHz. RTIF is a clearable, read-only status bit and is set when the output of the chosen (one-of-four selection) stage goes active. Clearing the RTIF is done by writing a one to RTFC. Writing has no effect on this bit. Reset clears RTIF.

#### TOFE — Timer Overflow Enable

When this bit is set, a CPU interrupt request is generated when the CTOF bit is set. Reset clears this bit.

#### RTIE — Real-Time Interrupt Enable

When this bit is set, a CPU interrupt request is generated when the RTIF bit is set. Reset clears this bit.

## TOFC — Timer Overflow Flag Clear

When a one is written to this bit, CTOF is cleared. Writing a zero has no effect on the CTOF bit. This bit always reads as zero.

## RTFC — Real-Time Interrupt Flag Clear

When a one is written to this bit, RTIF is cleared. Writing a zero has no effect on the RTIF bit. This bit always reads as zero.

## RT1–RT0 — Real-Time Interrupt Rate Select

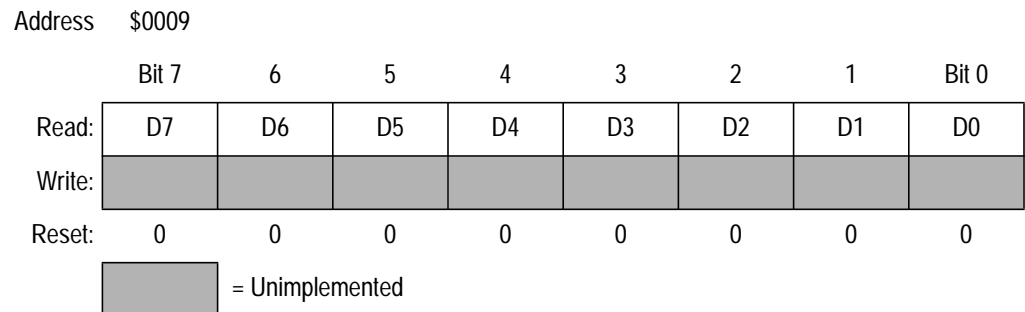
These two bits select one of four taps from the real-time interrupt circuit. Refer to [Table 8-1](#). Reset sets these two bits which selects the lowest periodic rate and gives the maximum time in which to alter these bits if necessary. Care should be taken when altering RT0 and RT1 if the timeout period is imminent or uncertain. If the selected tap is modified during a cycle in which the counter is switching, an RTIF could be missed or an additional one could be generated. To avoid problems, the COP should be cleared before changing RTI taps.

**Table 8-1. RTI and COP Rates at 4.096-MHz Oscillator**

RTI Rate 2.048-MHz Bus		RT1–RT0	Minimum COP Rates 2.048-MHz Bus		Maximum COP Rates 2.048-MHz Bus	
2 ms	$2^{12} \div E$	00	$(2^{15}-2^{12})/E$	14 ms	$(2^{15})/E$	16 ms
4 ms	$2^{13} \div E$	01	$(2^{16}-2^{13})/E$	28 ms	$(2^{16})/E$	32 ms
8 ms	$2^{14} \div E$	10	$(2^{17}-2^{14})/E$	56 ms	$(2^{17})/E$	64 ms
16 ms	$2^{15} \div E$	11	$(2^{18}-2^{15})/E$	112 ms	$(2^{18})/E$	128 ms

## 8.4 Core Timer Counter Register

The timer counter register is a read-only register that contains the current value of the 8-bit ripple counter at the beginning of the timer chain. This counter is clocked by the CPU clock (E/4) and can be used for various functions, including a software input capture. Extended time periods can be attained using the TOF function to increment a temporary RAM storage location, thereby simulating a 16-bit (or more) counter.



**Figure 8-3. Timer Counter Register (CTCR)**

The power-on cycle and the low-power reset both serve to clear the entire counter chain and begin clocking the counter. After 4064 cycles, the power-on/low-power reset circuit is released, which again clears the counter chain and allows the device to come out of reset. At this point, if  $\overline{\text{RESET}}$  is not asserted, the timer starts counting up from zero and normal device operation begins. When a reset other than POR and low-power reset is asserted any time during operation, the counter chain is cleared but the 4064-cycle stabilization period is not invoked.

## 8.5 Computer Operating Properly (COP) Reset

The COP watchdog timer function is implemented on this device by using the output of the RTI circuit and further dividing it by eight. The minimum COP reset rates are listed in [Figure 8-1](#). If the COP circuit times out, an internal reset is generated and the normal reset vector is fetched. Preventing a COP timeout, or clearing the COP is accomplished by writing a zero to bit 0 of address \$3FF0. When the COP is cleared, only the final divide-by-eight stage (output of the RTI) is cleared.

If the COP watchdog timer is allowed to time out, an internal reset is generated to reset the MCU.

The COP remains enabled after execution of the WAIT instruction and all associated operations apply. If the STOP instruction is disabled, execution of STOP instruction causes the CPU to enter wait mode just as if a wait mode instruction had been executed (except that when stop mode is exited, the COP timer is cleared). Thus, it is recommended that stop mode be disabled in devices that have the COP enabled, as this will prevent the COP from being disabled by the STOP instruction.

This COP's objective is to make it impossible for this device to become stuck or locked up and to be sure the COP is able to rescue the part from any situation where it might entrap itself in abnormal or unintended behavior. This function is a mask option.

### 8.6 Timer During Wait Mode

The CPU clock halts during wait mode, but the timer remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit wait mode. The COP is always enabled while in user mode.

## Section 9. Carrier Modulator Transmitter (CMT)

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### 9.2 Introduction

The carrier modulator transmitter (CMT) module provides a means to generate the protocol timing and carrier signals for a wide variety of encoding schemes. The CMT incorporates hardware to off-load the critical and/or lengthy timing requirements associated with code generation from the CPU, releasing much of its bandwidth to handle other tasks such as code data generation, data decompression, or keyboard scanning. The CMT does not include dedicated hardware configurations for specific protocols but is intended to be sufficiently programmable in its function to handle the timing requirements of most

protocols with minimal CPU intervention. When the modulator is disabled, certain CMT registers can be used to change the state of the infrared out pin (IRO) directly. This feature allows for the generation of future protocols not readily producible by the current architecture.

### 9.3 Overview

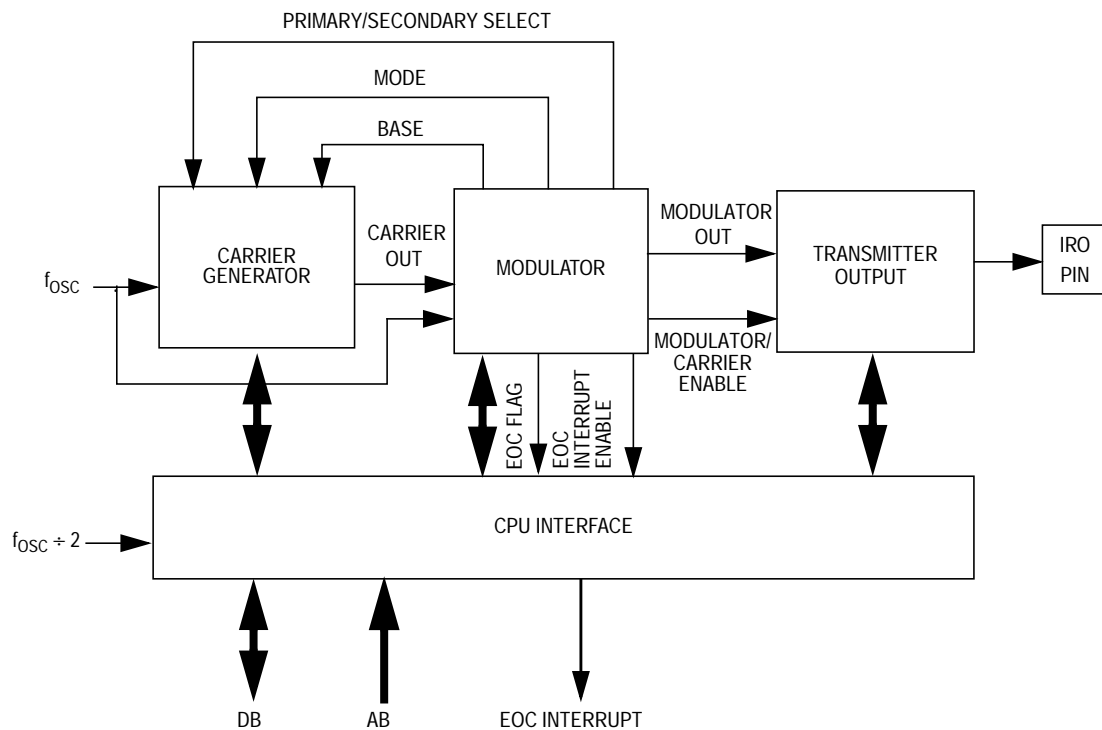
The module consists of carrier generator, modulator, and transmitter output blocks. The block diagram is shown in [Figure 9-1](#).

The carrier generator has a resolution of 500 ns with a 2-MHz oscillator. The user independently may define the high and low times of the carrier signal to determine both period and duty cycle. The carrier generator can generate signals with periods between 1  $\mu$ s (1 MHz) and 64  $\mu$ s (15.6 kHz) in steps of 500 ns. The possible duty cycle options will depend upon the number of counts required to complete the carrier period. For example, a 400-kHz signal has a period of 2.5  $\mu$ s and will therefore require 5 x 500 ns counts to generate. These counts may be split between high and low times so the duty cycles available will be 20% (one high, four low), 40% (two high, three low), 60% (three high, two low) and 80% (four high, one low). For lower frequency signals with larger periods, higher resolution (as a percentage of the total period) duty cycles are possible. The carrier generator may select between two sets of high and low times. When operating in normal mode (subsequently referred to as time mode), just one set will be used. When operating in FSK (frequency shift key) mode, the generator will toggle between the two sets when instructed to do so by the modulator, allowing the user to dynamically switch between two carrier frequencies without CPU intervention. When the BASE bit in the modulator control and status register (MCSR) is set, the carrier output to the modulator is held high continuously to allow for the generation of baseband protocols. See [9.4 Carrier Generator](#).

The modulator provides a simple method to control protocol timing. The modulator has a resolution of 4  $\mu$ s with a 2-MHz oscillator. It can count system clocks to provide real-time control or it can count carrier clocks for self-clocked protocols. The modulator can either gate the carrier onto the modulator output (TIME), control the logic level of the modulator

output (baseband), or directly route the carrier to the modulator output while providing a signal to switch the carrier generator between high/low time register buffers (FSK). See [9.5 Modulator](#).

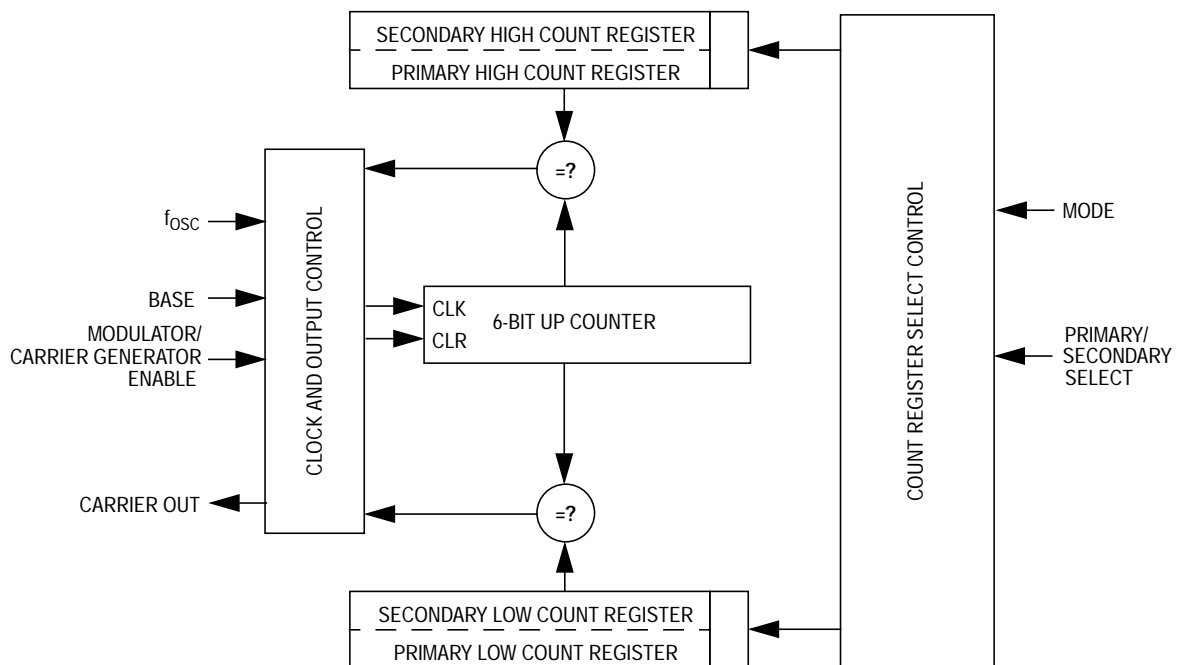
The transmitter output block controls the state of the infrared out pin (IRO). The modulator output is gated on to the IRO pin when the modulator/carrier generator is enabled. Otherwise, the IRO pin is controlled by the state of the IRO latch, which is directly accessible to the CPU by means of bit 7 of the carrier generator data registers CHR1 and CLR1. The IRO latch can be written to on either edge of the internal bus clock ( $f_{osc}/2$ ), allowing for IR waveforms which have a resolution of twice the bus clock frequency ( $f_{osc}$ ). See [9.4.2 Carrier Generator Data Registers \(CHR1, CLR1, CHR2, and CLR2\)](#).



**Figure 9-1. Carrier Modulator Transmitter Module Block Diagram**

## 9.4 Carrier Generator

The carrier signal is generated by counting a predetermined number of input clocks (500 ns for a 2-MHz oscillator) for both the carrier high time and the carrier low time. The period is determined by the total number of clocks counted. The duty cycle is determined by the ratio of high time clocks to total clocks counted. The high and low time values are user programmable and are held in two registers. An alternate set of high/low count values is held in another set of registers to allow the generation of dual frequency FSK (frequency shift keying) protocols without CPU intervention. The MCGEN bit in the MCSR must be set and the BASE bit in the MCSR must be cleared to enable carrier generator clocks. The block diagram is shown in [Figure 9-2](#).



**Figure 9-2. Carrier Generator Block Diagram**



### 9.4.1 Time Counter

The high/low time counter is a 6-bit up counter. After each increment, the contents of the counter are compared with the appropriate high or low count value register. When this value is reached, the counter is reset and the compare is redirected to the other count value register. Assuming that the high time count compare register is currently active, a valid compare will cause the carrier output to be driven low. The counter will continue to increment and when reaching the value stored in the selected low count value register, it will be cleared and will cause the carrier output to be driven high. The cycle repeats, automatically generating a periodic signal which is directed to the modulator. The lowest frequency (maximum period) and highest frequency (minimum period) which can be generated are defined as:

$$f_{\max} = f_{\text{osc}} \div (2 \times 1) \text{ Hz}$$

$$f_{\min} = f_{\text{osc}} \div (2 \times (2^6 - 1)) \text{ Hz}$$

In the general case, the carrier generator output frequency is:

$$f_{\text{out}} = f_{\text{osc}} \div (\text{Highcount} + \text{Lowcount}) \text{ Hz}$$

Where:  $0 < \text{Highcount} < 64$  and  
 $0 < \text{Lowcount} < 64$

**NOTE:** *These equations assume the DIV2 bit (bit 6) of the MCSR is clear. When the DIV2 bit is set, the carrier generator frequency will be half of what is shown in these equations.*

The duty cycle of the carrier signal is controlled by varying the ratio of high time to low + high time. As the input clock period is fixed, the duty cycle resolution will be proportional to the number of counts required to generate the desired carrier period.

$$\text{Duty Cycle} = \frac{\text{Highcount}}{\text{Highcount} + \text{Lowcount}}$$

# Carrier Modulator Transmitter (CMT)

## 9.4.2 Carrier Generator Data Registers (CHR1, CLR1, CHR2, and CLR2)

The carrier generator contains one 8-bit data register: primary high time (CHR1); one 7-bit data register: primary low time (CLR1); and two 6-bit data registers: secondary high time (CHR2) and secondary low time (CLR2). Bit 7 of CHR1 and CHR2 is used to read and write the IRO latch.

**CHR1** Address \$0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IROLN	CMPOL	PH5	PH4	PH3	PH2	PH1	PH0
Write:								
Reset:	0	0	U	U	U	U	U	U

U = Unaffected

**CLR1** Address \$0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IROLP	0	PL5	PL4	PL3	PL2	PL1	PL0
Write:								
Reset:	0	0	U	U	U	U	U	U

U = Unaffected

**CHR2** Address \$0012

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	SH5	SH4	SH3	SH2	SH1	SH0
Write:								
Reset:	0	0	U	U	U	U	U	U

U = Unaffected

**CLR2** Address \$0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	SL5	SL4	SL3	SL2	SL1	SL0
Write:								
Reset:	0	0	U	U	U	U	U	U

U = Unaffected

**Figure 9-3. Carrier Data Register (CHR1, CLR1, CHR2, and CLR2)**

### PH0–PH5 and PL0–PL5 — Primary Carrier High and Low Time Data Values

When selected, these bits contain the number of input clocks required to generate the carrier high and low time periods. When operating in time mode (see [9.5.1 Time Mode](#)), this register pair is always selected. When operating in FSK mode (see [9.5.2 FSK Mode](#)), this register pair and the secondary register pair are alternately selected under control of the modulator. The primary carrier high and low time values are undefined out of reset. These bits must be written to nonzero values before the carrier generator is enabled to avoid spurious results.

**NOTE:** *Writing to CHR1 to update PH0–PH5 or to CLR1 to update PL0–PL5 will also update the IRO latch. When MCGEN (bit 0 in the MCSR) is clear, the IRO latch value appears on the IRO output pin. Care should be taken that bit 7 of the data to be written to CHR1 or CHL1 should contain the desired state of the IRO latch.*

*Additionally, writing to CHR1 to update PH0–PH5 will also update the CMT polarity bit. Care should be taken that bit 6 of the data to be written to CHR1 should contain the desired state of the polarity bit.*

### SH0–SH5 and SL0–SL5 — Secondary Carrier High and Low Time Data Values

When selected, these bits contain the number of input clocks required to generate the carrier high and low time periods. When operating in time mode (see [9.5.1 Time Mode](#)), this register pair is never selected. When operating in FSK mode (see [9.5.2 FSK Mode](#)), this register pair and the primary register pair are alternately selected under control of the modulator. The secondary carrier high and low time values are undefined out of reset. These bits must be written to nonzero values before the carrier generator is enabled when operating in FSK mode.

### CMPOL — CMT output Polarity

This bit controls the polarity of the CMT output (IRO). When this bit is a zero, then the CMT output is active high. When this bit is set to one the CMT output is active low, in other words inverted. The reset state of this bit is zero.

### IROLN and IROLP — IRO Latch Control

Reading IROLN or IROLP reads the state of the IRO latch. Writing IROLN updates the IRO latch with the data being written on the negative edge of the internal processor clock ( $f_{osc}/2$ ). Writing IROLP updates the IRO latch on the positive edge of the internal processor clock; for example, one  $f_{osc}$  period later. The IRO latch is clear out of reset.

**NOTE:** *Writing to CHR1 to update IROLN or to CLR1 to update IROLP will also update the primary carrier high and low data values. Care should be taken that bits 5–0 of the data to be written to CHR1 or CHL1 should contain the desired values for the primary carrier high or low data.*

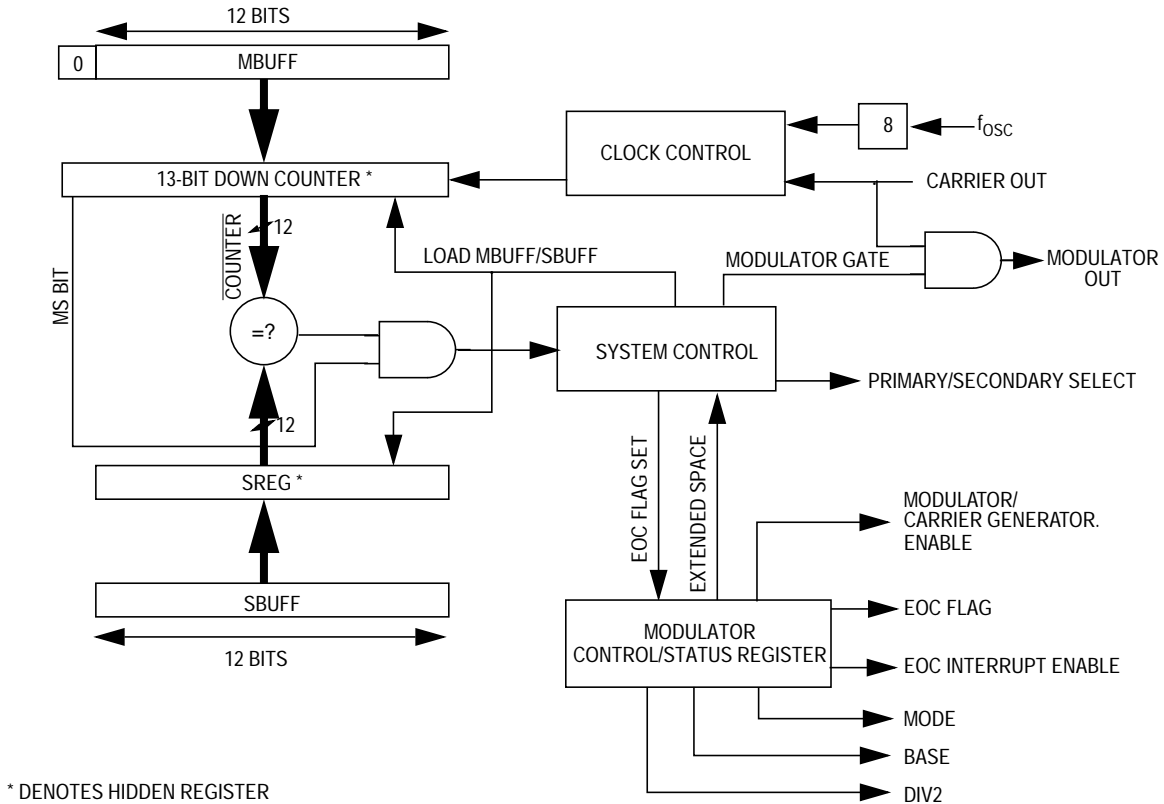
*In addition, writing to CHR1 to update IROLN will update the CMT polarity bit. Care should be taken that bit 6 of the data to be written to CHR1 should contain the desired values for the polarity bit.*

## 9.5 Modulator

The modulator consists of a 12-bit down counter with underflow detection which is loaded from the modulation mark period from the mark buffer register, MBUFF. When this counter underflows, the modulator gate is closed and a 12-bit comparator is enabled which continually compares the logical complement of the contents of the (still) decrementing counter with the contents of the modulation space period register, SREG. When a match is obtained, the modulator control gate is opened again. Should  $SREG = 0$ , the match will be immediate and no space period will be generated (for instance, for FSK protocols which require successive bursts of different frequencies). When the match occurs, the counter is reloaded with the contents of MBUFF, SREG is reloaded with the contents of its buffer, SBUFF, and the cycle repeats. The MCGEN bit in the MCSR must be set to enable the modulator timer. The 12-bit MBUFF and SBUFF registers are accessed through three 8-bit modulator period registers, MDR1, MDR2, and MDR3.

The modulator can operate in two modes, time and FSK. In time mode, the modulator counts clocks derived from the system oscillator and

modulates a single-carrier frequency or no carrier (baseband). In FSK mode, the modulator counts carrier periods and instructs the carrier generator to alternate between two carrier frequencies whenever a modulation period (mark + space counts) expires.



**Figure 9-4. Modulator Block Diagram**

### 9.5.1 Time Mode

When the modulator operates in time mode, the modulation mark and space periods consist of zero or an integer number of  $f_{osc} \div 8$  clocks (= 250 kHz @ 2 MHz osc). This provides a modulator resolution of 4  $\mu$ s and a maximum mark and space periods of about 16 ms (each). However, to prevent carrier glitches which could affect carrier spectral purity, the modulator control gate and carrier clock are synchronized. The carrier signal is activated when the modulator gate opens. The modulator gate can only close when the carrier signal is low (the output

## Carrier Modulator Transmitter (CMT)

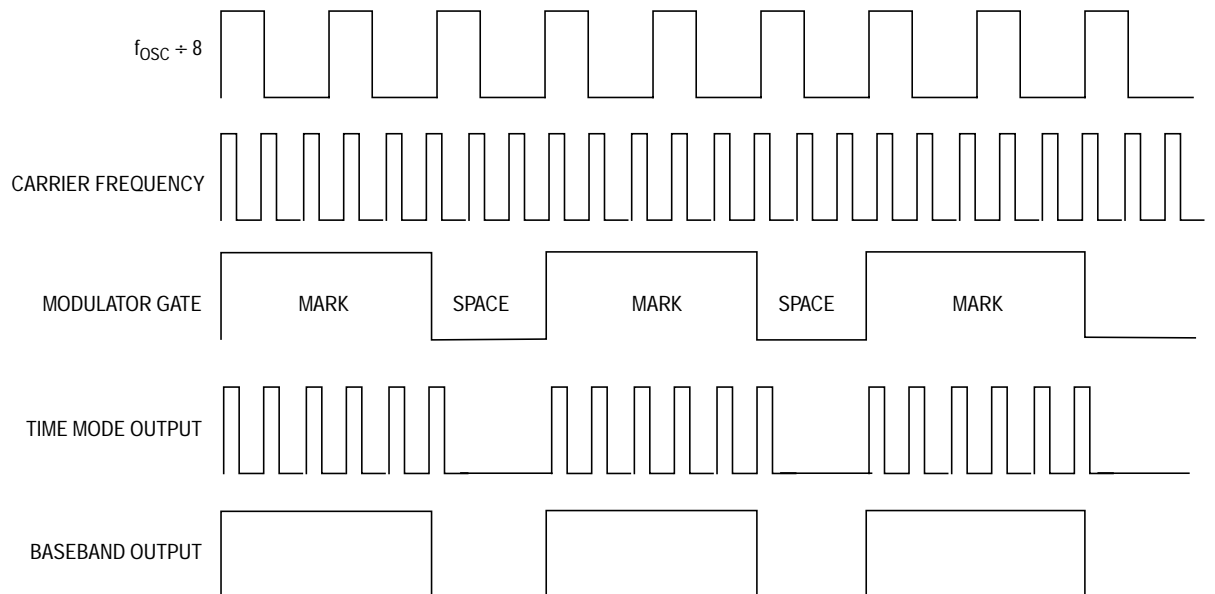
logic level during space periods is low). If the carrier generator is in baseband mode (BASE bit in MCSR is high), the modulator output will be at a logic 1 for the duration of the mark period and at a logic 0 for the duration of a space period. See [Figure 9-5](#).

The mark and space time equations are:

$$t_{\text{mark}} = \frac{(\text{MBUFF} + 1) \times 8}{f_{\text{osc}}} \text{secs}$$

$$t_{\text{space}} = \frac{\text{SBUFF} \times 8}{f_{\text{osc}}} \text{secs}$$

Setting the DIV2 bit in the MCSR will double mark and space times.



**Figure 9-5. CMT Operation in Time Mode**

## 9.5.2 FSK Mode

When the modulator operates in FSK mode, the modulation mark and space periods consist of an integer number of carrier clocks (space period can be zero). When the mark period expires, the space period is transparently started (as in time mode); however, in FSK mode the carrier switches between data registers in preparation for the next mark period. The carrier generator toggles between primary and secondary data register values whenever the modulator mark period expires. The space period provides an interpulse gap (no carrier), but if SBUFF = 0, then the modulator and carrier generator will switch between carrier frequencies without a gap or any carrier glitches (zero space).

Using timing data for carrier burst and interpulse gap length calculated by the CPU, FSK mode can automatically generate a phase-coherent, dual-frequency FSK signal with programmable burst and interburst gaps.

The mark and space time equations for FSK mode are:

$$t_{\text{mark}} = \frac{\text{MBUFF} + 1}{f_{\text{cg}}} \text{secs}$$

$$t_{\text{space}} = \frac{\text{SBUFF}}{f_{\text{cg}}} \text{secs}$$

Where  $f_{\text{cg}}$  is the frequency output from the carrier generator, setting the DIV2 bit in the MCSR will double mark and space times.

## 9.5.3 Extended Space Operation

In either time or FSK mode, the space period can be made longer than the maximum possible value of SBUFF. Setting the EXSPC bit in the MCSR will force the modulator to treat the next modulation period (beginning with the next load of MBUFF/SBUFF) as a space period equal in length to the mark and space counts combined. Subsequent modulation periods will consist entirely of these extended space periods with no mark periods. Clearing EXSPC will return the modulator to standard operation at the beginning of the next modulation period. To calculate the length of an extended space in time mode, use the equation:

$$t_{\text{espace}} = \frac{((\text{SBUFF}_1) + (\text{MBUFF}_2 + 1 + \text{SBUFF}_2) + \dots + (\text{MBUFF}_n + 1 + \text{SBUFF}_n)) \times 8}{f_{\text{osc}}} \text{ secs}$$

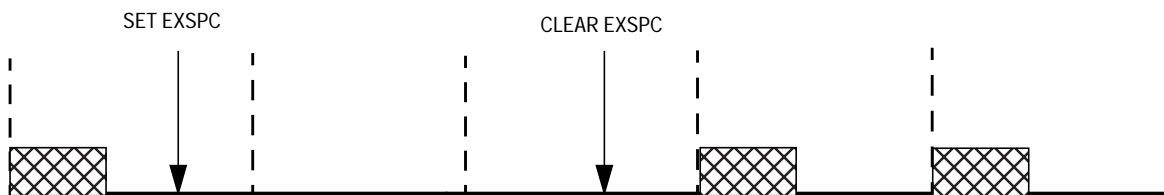
Where the subscripts 1, 2, ... n refer to the modulation periods that elapsed while the EXSPC bit was set.

Similarly, to calculate the length of an extended space in FSK mode, use the equation:

$$t_{\text{espace}} = \frac{((\text{SBUFF}_1) + (\text{MBUFF}_2 + 1 + \text{SBUFF}_2) + \dots + (\text{MBUFF}_n + 1 + \text{SBUFF}_n))}{f_{\text{cg}}} \text{ secs}$$

Where  $f_{\text{cg}}$  is the frequency output from the carrier generator. For an example of extended space operation, see [Figure 9-6](#).

**NOTE:** *The EXSPC feature can be used to emulate a zero mark event.*



**Figure 9-6. Extended Space Operation**

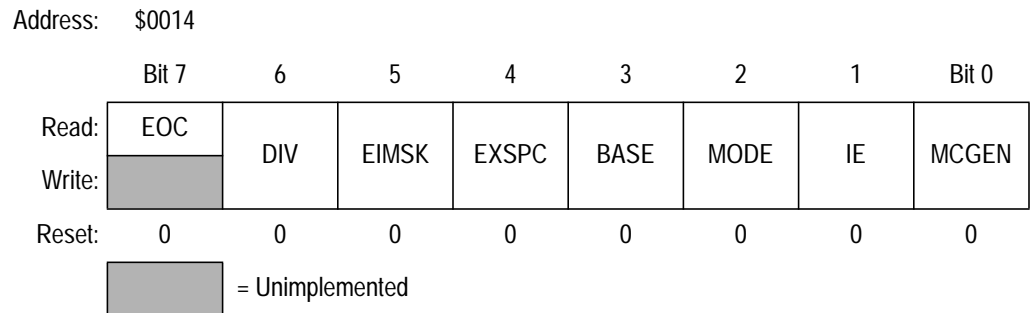


### 9.5.3.1 End Of Cycle (EOC) Interrupt

At the end of each cycle (when the counter is reloaded from MBUFF), the end of cycle (EOC) flag is set. If the interrupt enable bit was previously set, an interrupt will also be issued to the CPU. The EOC interrupt provides a means for the user to reload new mark/space values into the MBUFF and SBUFF registers. As the EOC interrupt is coincident with reloading the counter, MBUFF does not require additional buffering and may be updated with a new value for the next period from within the EOC interrupt service routine (ISR). To allow both mark and space period values to be updated from within the same ISR, SREG is buffered by SBUFF. The contents written to SBUFF are transferred to the active register SREG at the end of every cycle irrespective of the state of the EOC flag. The EOC flag is cleared by a read of the modulator control and status register (MCSR) followed by an access of MDR2 or MDR3. The EOC flag must be cleared within the ISR to prevent another interrupt being generated after exiting the ISR. If the EOC interrupt is not being used (IE = 0), the EOC flag need not be cleared.

### 9.5.3.2 Modulator Control and Status Register

The modulator control and status register (MCSR) contains the modulator and carrier generator enable (MCGEN), interrupt enable (IE), mode select (MODE), baseband enable (BASE), extended space (EXSPC), and external interrupt mask (EIMSK) control bits, divide-by-two prescaler (DIV2) bit, and the end of cycle (EOC) status bit.



**Figure 9-7. Modulator Control and Status Register (MCSR)**

### EOC — End Of Cycle Status Flag

1 = End of modulator cycle (counter = SBUFF) has occurred

0 = Current modulation cycle in progress

EOC is set when a match occurs between the contents of the space period register, SREG, and the down counter. This is recognized as the end of the modulation cycle. At this time, the counter is initialized with the (possibly new) contents of the mark period buffer, MBUFF, and the space period register, SREG, is loaded with the (possibly new) contents of the space period buffer, SBUFF. This flag is cleared by a read of the MCSR followed by an access of MDR2 or MDR3. The EOC flag is cleared by reset.

### DIV2 — Divide-by-two prescaler

1 = Divide-by-two prescaler enabled

0 = Divide-by-two prescaler disabled

The divide-by-two prescaler causes the CMT to be clocked at the bus rate when enabled and 2 x the bus rate when disabled ( $f_{osc}$ ). Since this bit is not double buffered, it should not be set during a transmission.

### EIMSK — External Interrupt Mask

1 = IRQ and keyscan interrupts masked

0 = IRQ and keyscan interrupts enabled

The external interrupt mask bit is used to mask IRQ and keyscan interrupts. This bit is cleared by reset.

### EXSPC — Extended Space Enable

1 = Extended space enabled

0 = Extended space disabled

For a description of the extended space enable bit, see [9.5.3 Extended Space Operation](#). This bit is cleared by reset.

**BASE** — Baseband Enable

- 1 = Baseband enabled
- 0 = Baseband disabled

When set, the BASE bit disables the carrier generator and forces the carrier output high for generation of baseband protocols. When BASE is clear, the carrier generator is enabled and the carrier output toggles at the frequency determined by values stored in the carrier data registers. See [9.5.1 Time Mode](#). This bit is cleared by reset. This bit is not double buffered and should not be written to during a transmission.

**MODE** — Mode Select

- 1 = CMT operates in FSK mode.
- 0 = CMT operates in Time mode.

For a description of CMT operation in time mode, see [9.5.1 Time Mode](#). For a description of CMT operation in FSK mode, see [9.5.2 FSK Mode](#). This bit is cleared by reset. This bit is not double buffered and should not be written to during a transmission.

**IE** — Interrupt Enable

- 1 = CPU interrupt enabled
- 0 = CPU interrupt disabled

A CPU interrupt will be requested when EOC is set if IE was previously set. If IE is clear, EOC will not request a CPU interrupt.

**MCGEN** — Modulator and Carrier Generator Enable

- 1 = Modulator and carrier generator enabled
- 0 = Modulator and carrier generator disabled

Setting MCGEN will initialize the carrier generator and modulator and will enable all clocks. Once enabled, the carrier generator and modulator will function continuously. When MCGEN is cleared, the current modulator cycle will be allowed to expire before all carrier and modulator clocks are disabled (to save power) and the modulator output is forced low. To prevent spurious operation, the user should initialize all data and control registers before enabling the system. This bit is cleared by reset.



## 9.6 Wait Mode Operation

During wait mode the CMT, if enabled, will continue to operate normally. However, there will be no new codes or changes of pattern mode while in wait mode, as the CPU is not operating. In addition, the CMT will not generate any new interrupts while the chip is in wait mode, although if it has one pending when wait mode is entered then that pending interrupt will serve to pull the chip out of WAIT mode.

**NOTE:** *Although the CMT will not generate any new interrupts while wait mode is active, a previously generated CMT interrupt that is still pending will bring the MCU out of wait mode.*

## 9.7 Stop Mode Operation

During stop mode, the CMT halts all operation. No registers are affected.



## Section 10. Instruction Set

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## 10.2 Introduction

The MCU instruction set has 62 instructions and uses eight addressing modes. The instructions include all those of the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is stored in the index register, and the low-order product is stored in the accumulator.

## 10.3 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. The addressing modes provide eight different ways for the CPU to find the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative



### 10.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

### 10.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

### 10.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses \$00 as the high byte of the operand address.

### 10.3.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

## 10.3.5 Indexed, No Offset

Indexed instructions with no offset are 1-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the effective address of the operand. The CPU automatically uses \$00 as the high byte, so these instructions can address locations \$0000–\$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or I/O location.

## 10.3.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are 2-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the effective address of the operand. These instructions can access locations \$0000–\$01FE.

Indexed 8-bit offset instructions are useful for selecting the *k*th element in an *n*-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 (\$01FE). The *k* value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

## 10.3.7 Indexed, 16-Bit Offset

Indexed, 16-bit offset instructions are 3-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset.

Indexed, 16-bit offset instructions are useful for selecting the *k*th element in an *n*-element table anywhere in memory.

As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

### 10.3.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the effective branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two's complement byte that gives a branching range of  $-128$  to  $+127$  bytes from the address of the next location after the branch instruction.

When using the Motorola assembler, the programmer does not need to calculate the offset, because the assembler determines the proper offset and verifies that it is within the span of the branch.

## 10.4 Instruction Types

The MCU instructions fall into the following five categories:

- Register/Memory Instructions
- Read-Modify-Write Instructions
- Jump/Branch Instructions
- Bit Manipulation Instructions
- Control Instructions

## 10.4.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

**Table 10-1. Register/Memory Instructions**

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

## 10.4.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

**NOTE:** *Do not use read-modify-write operations on write-only registers.*

**Table 10-2. Read-Modify-Write Instructions**

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR <sup>(1)</sup>
Bit Set	BSET <sup>(1)</sup>
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST <sup>(2)</sup>

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

## 10.4.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from  $-128$  to  $+127$  from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

**Table 10-3. Jump and Branch Instructions**

<b>Instruction</b>	<b>Mnemonic</b>
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{\text{IRQ}}$ Pin High	BIH
Branch if $\overline{\text{IRQ}}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

## 10.4.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

**Table 10-4. Bit Manipulation Instructions**

<b>Instruction</b>	<b>Mnemonic</b>
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET



### 10.4.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

**Table 10-5. Control Instructions**

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

## 10.5 Instruction Set Summary

**Table 10-6. Instruction Set Summary**

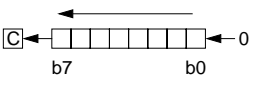
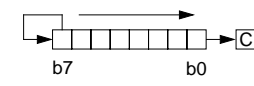
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #opr ADC opr ADC opr ADC opr,X ADC opr,X ADC ,X	Add with Carry	$A \leftarrow (A) + (M) + (C)$	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X	Add without Carry	$A \leftarrow (A) + (M)$	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X	Logical AND	$A \leftarrow (A) \wedge (M)$	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL opr ASLA ASLX ASL opr,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
ASR opr ASRA ASRX ASR opr,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff	5 3 3 6 5
BCC rel	Branch if Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? C = 0$	—	—	—	—	—	REL	24	rr	3
BCLR n opr	Clear Bit n	$M_n \leftarrow 0$	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS rel	Branch if Carry Bit Set (Same as BLO)	$PC \leftarrow (PC) + 2 + rel ? C = 1$	—	—	—	—	—	REL	25	rr	3
BEQ rel	Branch if Equal	$PC \leftarrow (PC) + 2 + rel ? Z = 1$	—	—	—	—	—	REL	27	rr	3
BHCC rel	Branch if Half-Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? H = 0$	—	—	—	—	—	REL	28	rr	3
BHCS rel	Branch if Half-Carry Bit Set	$PC \leftarrow (PC) + 2 + rel ? H = 1$	—	—	—	—	—	REL	29	rr	3
BHI rel	Branch if Higher	$PC \leftarrow (PC) + 2 + rel ? C \vee Z = 0$	—	—	—	—	—	REL	22	rr	3
BHS rel	Branch if Higher or Same	$PC \leftarrow (PC) + 2 + rel ? C = 0$	—	—	—	—	—	REL	24	rr	3

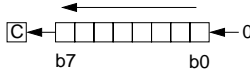
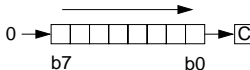
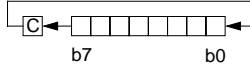
Table 10-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIH <i>rel</i>	Branch if IRQ Pin High	$PC \leftarrow (PC) + 2 + rel ? IRQ = 1$	—	—	—	—	—	REL	2F	rr	3
BIL <i>rel</i>	Branch if IRQ Pin Low	$PC \leftarrow (PC) + 2 + rel ? IRQ = 0$	—	—	—	—	—	REL	2E	rr	3
BIT # <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> ,X BIT <i>opr</i> ,X BIT ,X	Bit Test Accumulator with Memory Byte	$(A) \wedge (M)$	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO <i>rel</i>	Branch if Lower (Same as BCS)	$PC \leftarrow (PC) + 2 + rel ? C = 1$	—	—	—	—	—	REL	25	rr	3
BLS <i>rel</i>	Branch if Lower or Same	$PC \leftarrow (PC) + 2 + rel ? C \vee Z = 1$	—	—	—	—	—	REL	23	rr	3
BMC <i>rel</i>	Branch if Interrupt Mask Clear	$PC \leftarrow (PC) + 2 + rel ? I = 0$	—	—	—	—	—	REL	2C	rr	3
BMI <i>rel</i>	Branch if Minus	$PC \leftarrow (PC) + 2 + rel ? N = 1$	—	—	—	—	—	REL	2B	rr	3
BMS <i>rel</i>	Branch if Interrupt Mask Set	$PC \leftarrow (PC) + 2 + rel ? I = 1$	—	—	—	—	—	REL	2D	rr	3
BNE <i>rel</i>	Branch if Not Equal	$PC \leftarrow (PC) + 2 + rel ? Z = 0$	—	—	—	—	—	REL	26	rr	3
BPL <i>rel</i>	Branch if Plus	$PC \leftarrow (PC) + 2 + rel ? N = 0$	—	—	—	—	—	REL	2A	rr	3
BRA <i>rel</i>	Branch Always	$PC \leftarrow (PC) + 2 + rel ? 1 = 1$	—	—	—	—	—	REL	20	rr	3
BRCLR <i>n opr rel</i>	Branch if Bit n Clear	$PC \leftarrow (PC) + 2 + rel ? Mn = 0$	—	—	—	—	↑	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN <i>rel</i>	Branch Never	$PC \leftarrow (PC) + 2 + rel ? 1 = 0$	—	—	—	—	—	REL	21	rr	3
BRSET <i>n opr rel</i>	Branch if Bit n Set	$PC \leftarrow (PC) + 2 + rel ? Mn = 1$	—	—	—	—	↓	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET <i>n opr</i>	Set Bit n	$Mn \leftarrow 1$	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR <i>rel</i>	Branch to Subroutine	$PC \leftarrow (PC) + 2$ ; push (PCL) $SP \leftarrow (SP) - 1$ ; push (PCH) $SP \leftarrow (SP) - 1$ $PC \leftarrow (PC) + rel$	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	$C \leftarrow 0$	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	$I \leftarrow 0$	—	0	—	—	—	INH	9A		2

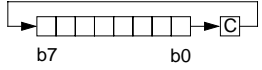
**Table 10-6. Instruction Set Summary (Continued)**

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR <i>opr</i> CLRA CLR X CLR <i>opr</i> ,X CLR ,X	Clear Byte	M ← \$00 A ← \$00 X ← \$00 M ← \$00 M ← \$00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff	5 3 3 6 5
CMP # <i>opr</i> CMP <i>opr</i> CMP <i>opr</i> CMP <i>opr</i> ,X CMP <i>opr</i> ,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff	2 3 4 5 4 3
COM <i>opr</i> COMA COM X COM <i>opr</i> ,X COM ,X	Complement Byte (One's Complement)	M ← (M̄) = \$FF – (M) A ← (Ā) = \$FF – (A) X ← (X̄) = \$FF – (X) M ← (M̄) = \$FF – (M) M ← (M̄) = \$FF – (M)	—	—	↑	↑	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff	5 3 3 6 5
CPX # <i>opr</i> CPX <i>opr</i> CPX <i>opr</i> CPX <i>opr</i> ,X CPX <i>opr</i> ,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff	2 3 4 5 4 3
DEC <i>opr</i> DECA DEC X DEC <i>opr</i> ,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↑	↑	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff	5 3 3 6 5
EOR # <i>opr</i> EOR <i>opr</i> EOR <i>opr</i> EOR <i>opr</i> ,X EOR <i>opr</i> ,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff	2 3 4 5 4 3
INC <i>opr</i> INCA INC X INC <i>opr</i> ,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↑	↑	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff	5 3 3 6 5
JMP <i>opr</i> JMP <i>opr</i> JMP <i>opr</i> ,X JMP <i>opr</i> ,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2

Table 10-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JSR <i>opr</i> JSR <i>opr</i> JSR <i>opr,X</i> JSR <i>opr,X</i> JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA # <i>opr</i> LDA <i>opr</i> LDA <i>opr</i> LDA <i>opr,X</i> LDA <i>opr,X</i> LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX # <i>opr</i> LDX <i>opr</i> LDX <i>opr</i> LDX <i>opr,X</i> LDX <i>opr,X</i> LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL <i>opr</i> LSLA LSLX LSL <i>opr,X</i> LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
LSR <i>opr</i> LSRA LSRX LSR <i>opr,X</i> LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG <i>opr</i> NEGA NEGX NEG <i>opr,X</i> NEG ,X	Negate Byte (Two's Complement)	M ← -(M) = \$00 - (M) A ← -(A) = \$00 - (A) X ← -(X) = \$00 - (X) M ← -(M) = \$00 - (M) M ← -(M) = \$00 - (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA # <i>opr</i> ORA <i>opr</i> ORA <i>opr</i> ORA <i>opr,X</i> ORA <i>opr,X</i> ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL <i>opr</i> ROLA ROLX ROL <i>opr,X</i> ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff	5 3 3 6 5

## Table 10-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR <i>opr</i> RORA RORX ROR <i>opr,X</i> ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd  ff	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← \$00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr,X</i> SBC <i>opr,X</i> SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA <i>opr</i> STA <i>opr</i> STA <i>opr,X</i> STA <i>opr,X</i> STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX <i>opr</i> STX <i>opr</i> STX <i>opr,X</i> STX <i>opr,X</i> STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff	4 5 6 5 4
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr,X</i> SUB <i>opr,X</i> SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2

**Table 10-6. Instruction Set Summary (Continued)**

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
TST <i>opr</i> TSTA TSTX TST <i>opr</i> ,X TST ,X	Test Memory Byte for Negative or Zero	(M) – \$00	—	—	↓	↓	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff	4 3 3 5 4
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0	—	—	—	INH	8F		2

- |          |   |            |                                      |
|----------|---|------------|--------------------------------------|
| A        | Accumulator   | <i>opr</i> | Operand (one or two bytes)           |
| C        | Carry/borrow flag   | PC         | Program counter                      |
| CCR      | Condition code register   | PCH        | Program counter high byte            |
| dd       | Direct address of operand   | PCL        | Program counter low byte             |
| dd rr    | Direct address of operand and relative offset of branch instruction | REL        | Relative addressing mode             |
| DIR      | Direct addressing mode  | <i>rel</i> | Relative program counter offset byte |
| ee ff    | High and low bytes of offset in indexed, 16-bit offset addressing   | rr         | Relative program counter offset byte |
| EXT      | Extended addressing mode  | SP         | Stack pointer                        |
| ff       | Offset byte in indexed, 8-bit offset addressing                     | X          | Index register                       |
| H        | Half-carry flag   | Z          | Zero flag                            |
| hh ll    | High and low bytes of operand address in extended addressing        | #          | Immediate value                      |
| I        | Interrupt mask  | ^          | Logical AND                          |
| ii       | Immediate operand byte  | ∨          | Logical OR                           |
| IMM      | Immediate addressing mode   | ⊕          | Logical EXCLUSIVE OR                 |
| INH      | Inherent addressing mode  | ( )        | Contents of                          |
| IX       | Indexed, no offset addressing mode                                  | -( )       | Negation (two's complement)          |
| IX1      | Indexed, 8-bit offset addressing mode                               | ←          | Loaded with                          |
| IX2      | Indexed, 16-bit offset addressing mode                              | ?          | If                                   |
| M        | Memory location   | :          | Concatenated with                    |
| N        | Negative flag   | ↓          | Set or cleared                       |
| <i>n</i> | Any bit   | —          | Not affected                         |

Table 10-7. Opcode Map

MSB LSB	Bit Manipulation		Branch	Read-Modify-Write				Control		Register/Memory						MSB LSB		
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1		IX	
0	5 3 BRSET0 DIR	5 2 BSET0 DIR	3 2 BRA REL	5 2 NEG DIR	3 1 NEGA INH	3 1 NEGX INH	6 2 NEG IX1	5 1 NEG IX	9 1 RTI INH		2 2 SUB IMM	3 2 SUB DIR	4 3 SUB EXT	5 3 SUB IX2	4 2 SUB IX1	3 1 SUB IX	0	
1	5 3 BRCLR0 DIR	5 2 BCLR0 DIR	3 2 BRN REL						6 1 RTS INH		2 2 CMP IMM	3 2 CMP DIR	4 3 CMP EXT	5 3 CMP IX2	4 2 CMP IX1	3 1 CMP IX	1	
2	5 3 BRSET1 DIR	5 2 BSET1 DIR	3 2 BHI REL		11 1 MUL INH						2 2 SBC IMM	3 2 SBC DIR	4 3 SBC EXT	5 3 SBC IX2	4 2 SBC IX1	3 1 SBC IX	2	
3	5 3 BRCLR1 DIR	5 2 BCLR1 DIR	3 2 BLS REL	5 2 COM DIR	3 1 COMA INH	3 1 COMX INH	6 2 COM IX1	5 1 COM IX	10 1 SWI INH		2 2 CPX IMM	3 2 CPX DIR	4 3 CPX EXT	5 3 CPX IX2	4 2 CPX IX1	3 1 CPX IX	3	
4	5 3 BRSET2 DIR	5 2 BSET2 DIR	3 2 BCC REL	5 2 LSR DIR	3 1 LSRA INH	3 1 LSRX INH	6 2 LSR IX1	5 1 LSR IX			2 2 AND IMM	3 2 AND DIR	4 3 AND EXT	5 3 AND IX2	4 2 AND IX1	3 1 AND IX	4	
5	5 3 BRCLR2 DIR	5 2 BCLR2 DIR	3 2 BCS/BLO REL								2 2 BIT IMM	3 2 BIT DIR	4 3 BIT EXT	5 3 BIT IX2	4 2 BIT IX1	3 1 BIT IX	5	
6	5 3 BRSET3 DIR	5 2 BSET3 DIR	3 2 BNE REL	5 2 ROR DIR	3 1 RORA INH	3 1 RORX INH	6 2 ROR IX1	5 1 ROR IX			2 2 LDA IMM	3 2 LDA DIR	4 3 LDA EXT	5 3 LDA IX2	4 2 LDA IX1	3 1 LDA IX	6	
7	5 3 BRCLR3 DIR	5 2 BCLR3 DIR	3 2 BEQ REL	5 2 ASR DIR	3 1 ASRA INH	3 1 ASRX INH	6 2 ASR IX1	5 1 ASR IX		2 1 TAX INH		4 2 STA DIR	5 3 STA EXT	6 3 STA IX2	5 2 STA IX1	4 1 STA IX	7	
8	5 3 BRSET4 DIR	5 2 BSET4 DIR	3 2 BHCC REL	5 2 ASL/LSL DIR	3 1 ASLA/SLA INH	3 1 ASLX/SLX INH	6 2 ASL/LSL IX1	5 1 ASL/LSL IX		2 1 CLC INH	2 2 EOR IMM	3 2 EOR DIR	4 3 EOR EXT	5 3 EOR IX2	4 2 EOR IX1	3 1 EOR IX	8	
9	5 3 BRCLR4 DIR	5 2 BCLR4 DIR	3 2 BHCS REL	5 2 ROL DIR	3 1 ROLA INH	3 1 ROLX INH	6 2 ROL IX1	5 1 ROL IX		2 1 SEC INH	2 2 ADC IMM	3 2 ADC DIR	4 3 ADC EXT	5 3 ADC IX2	4 2 ADC IX1	3 1 ADC IX	9	
A	5 3 BRSET5 DIR	5 2 BSET5 DIR	3 2 BPL REL	5 2 DEC DIR	3 1 DECA INH	3 1 DECX INH	6 2 DEC IX1	5 1 DEC IX		2 1 CLI INH	2 2 ORA IMM	3 2 ORA DIR	4 3 ORA EXT	5 3 ORA IX2	4 2 ORA IX1	3 1 ORA IX	A	
B	5 3 BRCLR5 DIR	5 2 BCLR5 DIR	3 2 BMI REL							2 1 SEI INH	2 2 ADD IMM	3 2 ADD DIR	4 3 ADD EXT	5 3 ADD IX2	4 2 ADD IX1	3 1 ADD IX	B	
C	5 3 BRSET6 DIR	5 2 BSET6 DIR	3 2 BMC REL	5 2 INC DIR	3 1 INCA INH	3 1 INCX INH	6 2 INC IX1	5 1 INC IX		2 1 RSP INH		2 2 JMP DIR	3 3 JMP EXT	4 3 JMP IX2	3 2 JMP IX1	2 1 JMP IX	C	
D	5 3 BRCLR6 DIR	5 2 BCLR6 DIR	3 2 BMS REL	4 2 TST DIR	3 1 TSTA INH	3 1 TSTX INH	5 2 TST IX1	4 1 TST IX		2 1 NOP INH	6 2 BSR REL	5 2 JSR DIR	6 3 JSR EXT	7 3 JSR IX2	6 2 JSR IX1	5 1 JSR IX	D	
E	5 3 BRSET7 DIR	5 2 BSET7 DIR	3 2 BIL REL						2 1 STOP INH		2 2 LDX IMM	3 2 LDX DIR	4 3 LDX EXT	5 3 LDX IX2	4 2 LDX IX1	3 1 LDX IX	E	
F	5 3 BRCLR7 DIR	5 2 BCLR7 DIR	3 2 BIH REL	5 2 CLR DIR	3 1 CLRA INH	3 1 CLR INH	6 2 CLR IX1	5 1 CLR IX		2 1 WAIT INH	2 2 TXA INH		5 2 STX DIR	6 3 STX EXT	5 2 STX IX2	4 1 STX IX1	3 1 STX IX	F

INH = Inherent  
 IMM = Immediate  
 DIR = Direct  
 EXT = Extended  
 REL = Relative  
 IX = Indexed, No Offset  
 IX1 = Indexed, 8-Bit Offset  
 IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB LSB	0
0	5 3 BRSET0 DIR

MSB of Opcode in Hexadecimal  
 Number of Cycles  
 Opcode Mnemonic  
 Number of Bytes/Addressing Mode



## Section 11. Electrical Specifications

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### 11.2 Introduction

This section contains MCU electrical specifications and timing information.

## 11.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep  $V_{IN}$  and  $V_{OUT}$  within the range  $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$ . Connect unused inputs to the appropriate voltage level, either  $V_{SS}$  or  $V_{DD}$ .

Rating	Symbol	Value	Unit
Supply Voltage	$V_{DD}$	-0.3 to +7.0	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Current Drain Per Pin Excluding $V_{DD}$ and $V_{SS}$	I	25	mA
Operating Temperature Range MC68HC05RC18 (Standard)	$T_A$	$T_L$ to $T_H$ 0 to +70	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C

**NOTE:** *This device is not guaranteed to operate properly at the maximum ratings. Refer to [11.6 DC Electrical Characteristics \(5.0 Vdc\)](#) and [11.7 DC Electrical Characteristics \(2.2 Vdc\)](#) for guaranteed operating conditions.*

## 11.4 Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating Temperature Range MC68HC05RC18 (Standard)	$T_A$	$T_L$ to $T_H$ 0 to +70	°C

## 11.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance PDIP SOIC	$\theta_{JA}$	60 60	°C/W

# Electrical Specifications

## 11.6 DC Electrical Characteristics (5.0 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage $I_{LOAD} = 10.0 \mu A$ $I_{LOAD} = -10.0 \mu A$	$V_{OL}$ $V_{OH}$	— $V_{DD} - 0.1$	— —	0.1 —	V
Output High Voltage ( $I_{LOAD} = -4 \text{ mA}$ ) Port A, Port B, Port C (Bits 4–7) ( $I_{LOAD} = -20 \text{ mA}$ ) IRO ( $I_{LOAD} = -4 \text{ mA}$ ) Port C (Bits 0–3)	$V_{OH}$	$V_{DD} - 0.8$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	$V_{DD} - 0.2$ $V_{DD} - 0.4$ $V_{DD} - 0.2$	— — —	V
Output Low Voltage ( $I_{LOAD} = 6 \text{ mA}$ ) Port A, Port B, Port C (Bits 4–7) ( $I_{LOAD} = 35 \text{ mA}$ ) IRO ( $I_{LOAD} = 20 \text{ mA}$ ) Port C (Bits 0–3)	$V_{OL}$	— — —	0.2 0.4 0.2	0.5 0.8 0.5	V
Input High Voltage Port A, Port B, Port C, $\overline{IRQ}$ , $\overline{RESET}$ , $\overline{LPRST}$ , OSC1	$V_{IH}$	$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input Low Voltage Port A, Port B, Port C, $\overline{IRQ}$ , $\overline{RESET}$ , $\overline{LPRST}$ , OSC1	$V_{IL}$	$V_{SS}$	—	$0.2 \times V_{DD}$	V
Supply Current (see Notes) Run Wait Stop 25 °C 0 °C to +70 °C	$I_{DD}$	— — — —	2.4 0.3 0.5 0.5	4.0 1.0 10.0 20.0	mA mA $\mu A$ $\mu A$
I/O Ports Hi-Z Leakage Current Port A, Port B, Port C	$I_{OZ}$	-10	—	10	$\mu A$
Input Current $\overline{RESET}$ , $\overline{LPRST}$ , $\overline{IRQ}$ , OSC1 PB0–PB7 with Strong Pullups Enabled ( $V_{IN} = 0.2 \times V_{DD}$ ) <sup>9</sup> PB0–PB7 with Strong Pullups Enabled ( $V_{IN} = 0.7 \times V_{DD}$ ) PB0–PB7 with Weak Pullups Enabled ( $V_{IN} = 0.2 \times V_{DD}$ ) PB0–PB7 with Weak Pullups Enabled ( $V_{IN} = 0.7 \times V_{DD}$ )	$I_{IN}$	-1 -70 -40 -15 -5	— -136 -79 -48 -20	1 -210 -130 -80 -60	$\mu A$
Capacitance Ports (as Input or Output) $\overline{RESET}$ , $\overline{LPRST}$ , $\overline{IRQ}$	$C_{OUT}$ $C_{INT}$	— —	— —	12 8	pF

### NOTES:

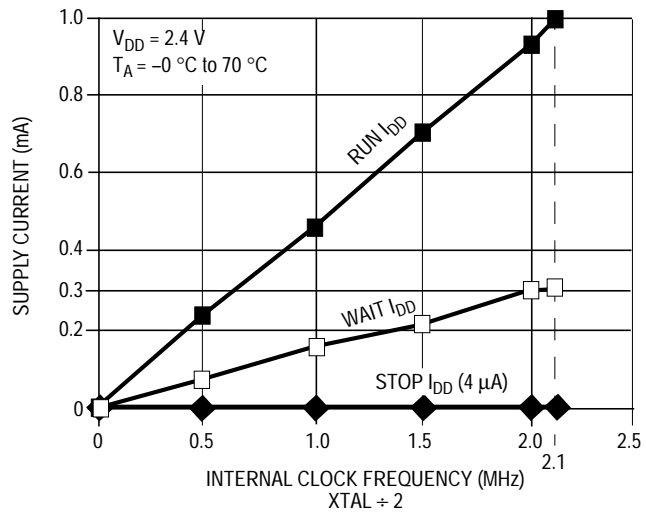
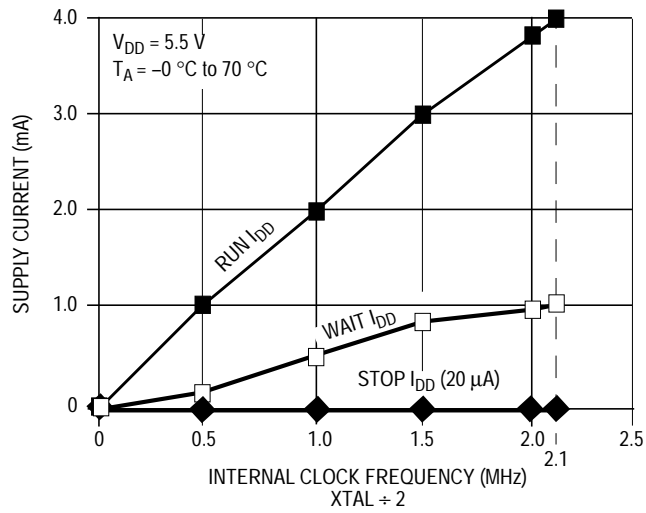
- $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = 0 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ , unless otherwise noted
- All values shown reflect average measurements.
- Typical values at midpoint of voltage range, 25 °C only
- Wait  $I_{DD}$ : only core timer active
- Run (Operating)  $I_{DD}$ , Wait  $I_{DD}$ : Measured using external square wave clock source ( $f_{OSC} = 4.2 \text{ MHz}$ ), all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs;  $C_L = 20 \text{ pF}$  on OSC2
- Wait, Stop  $I_{DD}$ : all ports configured as inputs,  $V_{IL} = 0.2 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.2 \text{ V}$
- Stop  $I_{DD}$  is measured with  $OSC1 = V_{SS}$ .
- Wait  $I_{DD}$  is affected linearly by the OSC2 capacitance.
- Strong pullups are designed to be capable of pulling to  $V_{IH}$  within 1  $\mu s$  for a 100 pF, 4-k $\Omega$  load.

## 11.7 DC Electrical Characteristics (2.2 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage $I_{LOAD} = 10.0 \mu A$ $I_{LOAD} = -10.0 \mu A$	$V_{OL}$ $V_{OH}$	— $V_{DD} - 0.1$	— —	0.1 —	V
Output High Voltage ( $I_{LOAD} = -1.2 \text{ mA}$ ) Port A, Port B, Port C (Bits 4–7) ( $I_{LOAD} = -6 \text{ mA}$ ) IRO ( $I_{LOAD} = -1.2 \text{ mA}$ ) Port C (Bits 0–3)	$V_{OH}$	$V_{DD} - 0.3$ $V_{DD} - 0.8$ $V_{DD} - 0.3$	$V_{DD} - 0.1$ $V_{DD} - 0.3$ $V_{DD} - 0.1$	— — —	V
Output Low Voltage ( $I_{LOAD} = 2.0 \text{ mA}$ ) Port A, Port B, Port C (Bits 4–7) ( $I_{LOAD} = 11 \text{ mA}$ ) IRO ( $I_{LOAD} = 7.0 \text{ mA}$ ) Port C (Bits 0–3)	$V_{OL}$	— — —	0.1 0.2 0.1	0.3 0.8 0.3	V
Input High Voltage Port A, Port B, Port C, $\overline{IRQ}$ , $\overline{RESET}$ , $\overline{LPRST}$ , OSC1	$V_{IH}$	$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input Low Voltage Port A, Port B, Port C, $\overline{IRQ}$ , $\overline{RESET}$ , $\overline{LPRST}$ , OSC1	$V_{IL}$	$V_{SS}$	—	$0.2 \times V_{DD}$	V
Supply Current (see Notes) Run Wait Stop 25 °C 0 °C to +70 °C	$I_{DD}$ $I_{DD}$ $I_{DD}$ $I_{DD}$	— — — —	0.75 0.1 0.1 0.1	1.0 0.3 1.0 4.0	mA mA $\mu A$ $\mu A$
I/O Ports Hi-Z Leakage Current Port A, Port B, Port C	$I_{OZ}$	-4	—	4	$\mu A$
Input Current $\overline{RESET}$ , $\overline{LPRST}$ , $\overline{IRQ}$ , OSC1 PB0–PB7 with Strong Pullups Enabled ( $V_{IN} = 0.4 \times V_{DD}$ ) <sup>9</sup> PB0–PB7 with Strong Pullups Enabled ( $V_{IN} = 0.7 \times V_{DD}$ ) PB0–PB7 with Weak Pullups Enabled ( $V_{IN} = 0.4 \times V_{DD}$ ) PB0–PB7 with Weak Pullups Enabled ( $V_{IN} = 0.7 \times V_{DD}$ )	$I_{IN}$	-0.4 -8 -5 -2 -1	— -21 -16 -6 -2	0.4 -35 -28 -15 -12	$\mu A$
Capacitance Ports (as Input or Output) $\overline{RESET}$ , $\overline{LPRST}$ , $\overline{IRQ}$	$C_{OUT}$ $C_{INT}$	— —	— —	12 8	pF

**NOTES:**

- $V_{DD} = 2.2 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = 0 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ , unless otherwise noted
- All values shown reflect average measurements.
- Typical values at midpoint of voltage range, 25 °C only
- Wait  $I_{DD}$ : only core timer active
- Run (Operating)  $I_{DD}$ , Wait  $I_{DD}$ : Measured using external square wave clock source ( $f_{OSC} = 4.2 \text{ MHz}$ ), all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs;  $C_L = 20 \text{ pF}$  on OSC2
- Wait, Stop  $I_{DD}$ : all ports configured as inputs,  $V_{IL} = 0.2 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.2 \text{ V}$
- Stop  $I_{DD}$  is measured with OSC1 =  $V_{SS}$ .
- Wait  $I_{DD}$  is affected linearly by the OSC2 capacitance.
- Strong pullups are designed to be capable of pulling to  $V_{IH}$  within 25  $\mu\text{s}$  for a 100 pF, 4-k $\Omega$  load.



**Figure 11-1. Maximum Supply Current versus Internal Clock Frequency**

## 11.8 Control Timing (2.2 Vdc to 5.0 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal	$f_{OSC}$	—	4.2	MHz
External Clock	$f_{OSC}$	dc	4.2	MHz
Internal Operating Frequency Crystal ( $f_{OSC} / 2$ )	$f_{OP}$	—	2.1	MHz
External Clock ( $f_{OSC} / 2$ )	$f_{OP}$	dc	2.1	MHz
Cycle Time	$t_{CYC}$	480	—	ns
Crystal Oscillator Startup Time (see Note 3)	$t_{OXOV}$	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator) ( see Note 3)	$t_{ILCH}$	—	100	ms
RESET Pulse Width	$t_{RL}$	1.5	—	$t_{CYC}$
Interrupt Pulse Width Low (Edge-Triggered)	$t_{ILIH}$	125	—	ns
Interrupt Pulse Period	$t_{ILIL}$	see Note 2	—	$t_{CYC}$
OSC1 Pulse Width	$t_{OH}, t_{OL}$	90	—	ns

NOTES:

1.  $V_{DD} = 2.2$  to  $5.5$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = 0$  °C to  $+70$  °C, unless otherwise noted
2. The minimum period,  $t_{ILIL}$ , should not be less than the number of cycle times it takes to execute the interrupt service routine plus  $19 t_{CYC}$ .
3. These features, are not tested.





## Section 12. Mechanical Specifications

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### 12.2 Introduction

This section describes the dimensions of the dual-in-line package (DIP), small outline integrated circuit (SOIC), and plastic leaded chip carrier (PLCC) MCU packages.

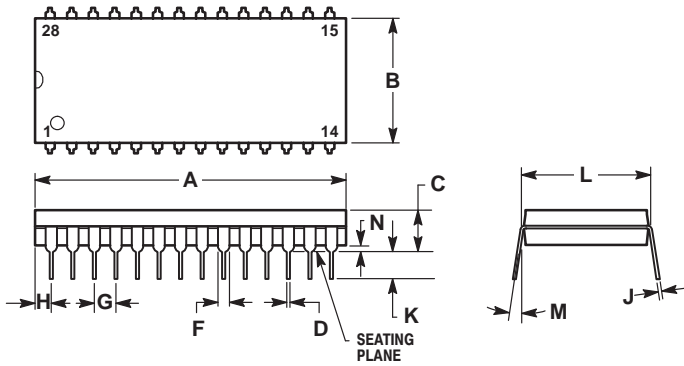
The following figures show the latest packages at the time of this publication. To make sure that you have the latest package specifications, contact one of the following:

- Local Motorola Sales Office
- Motorola Mfax
  - Phone 602-244-6609
  - EMAIL [rmfax0@email.sps.mot.com](mailto:rmfax0@email.sps.mot.com)
- Worldwide Web (wwweb) at <http://design-net.com>

Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.

# Mechanical Specifications

## 12.3 28-Pin Plastic Dual-In-Line Package (Case 710-02)

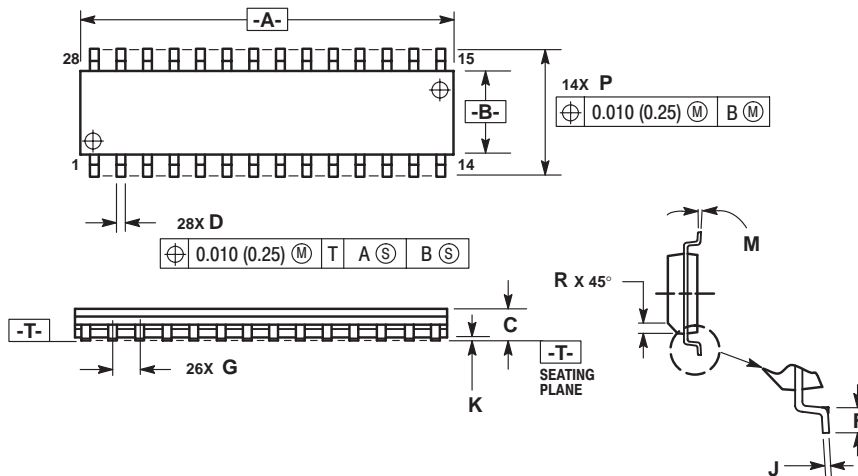


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

## 12.4 28-Pin Small Outline Integrated Circuit Package (Case 751F-04)

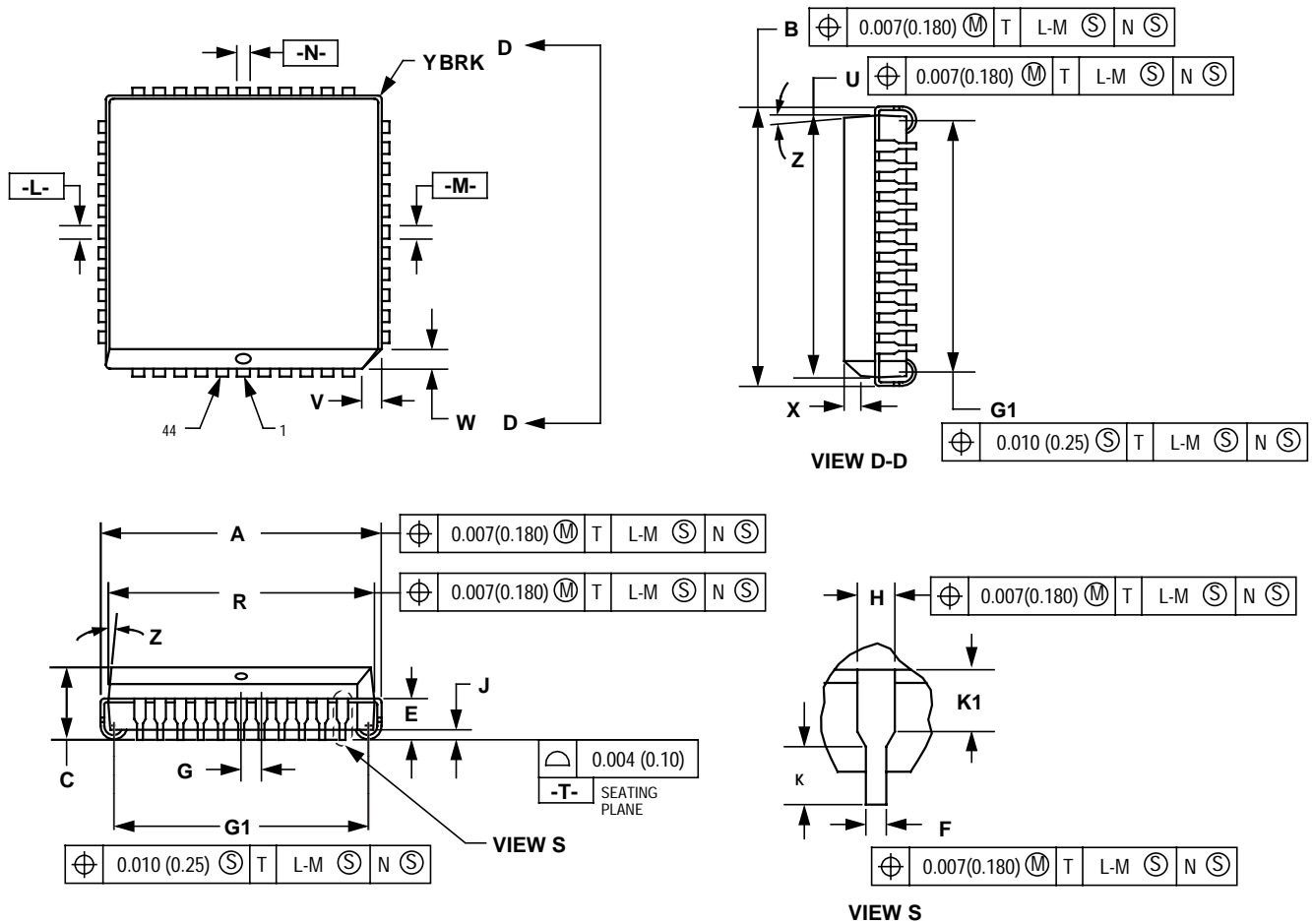


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

## 12.5 44-Pin Plastic Leaded Chip Carrier Package (Case 777-02)



**NOTES:**

- DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDERS EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSION R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF THE MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940116). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—



## Section 13. Ordering Information

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### 13.2 Introduction

This section contains instructions for ordering custom-masked ROM MCUs.

### 13.3 MCU Ordering Forms

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Motorola representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Motorola sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Motorola specification for the MCU
- Customer's application program on one of the media listed in [13.4 Application Program Media](#)

The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters. Then press the return key to start the BBS software.

### 13.4 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh<sup>®1</sup> 3 1/2-inch diskette (double-sided 800 K or double-sided high-density 1.4 M)
- MS-DOS<sup>®2</sup> or PC-DOS<sup>™3</sup> 3 1/2-inch diskette (double-sided 720 K or double-sided high-density 1.44 M)
- MS-DOS<sup>®</sup> or PC-DOS<sup>™</sup> 5 1/4-inch diskette (double-sided double-density 360 K or double-sided high-density 1.2 M)

Use positive logic for data and addresses.

When submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

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1. Macintosh is a registered trademark of Apple Computer, Inc.  
2. MS-DOS is a registered trademark of Microsoft Corporation.  
3. PC-DOS is a trademark of International Business Machines Corporation.

**NOTE:** *Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. Write \$00 in all non-user ROM locations or leave all nonuser ROM locations blank. Refer to the current MCU ordering form for additional requirements. Motorola may request pattern re-submission if nonuser areas contain any nonzero code.*

If the memory map has two user ROM areas with the same addresses, then write the two areas in separate files on the diskette. Label the diskette with both filenames.

In addition to the object code, a file containing the source code can be included. Motorola keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the filename of the source code.

## 13.5 ROM Program Verification

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program and then submits the MCU order along with the application program.

Motorola inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain nonuser ROM code, such as self-check code. Motorola sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Motorola will program the listing verify file into customer-supplied blank preformatted Macintosh or DOS disks. All original pattern media are filed for contractual purposes and are not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Motorola. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

## 13.6 ROM Verification Units (RVUs)

After receiving the signed listing verify form, Motorola manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Motorola then produces 10 MCUs, called RVUs, and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented. The 10 RVUs are free of charge with the minimum order quantity. These units are not to be used for qualification or production. RVUs are not guaranteed by Motorola Quality Assurance.

## 13.7 MC Order Numbers

**Table 13-1** shows the MC order numbers for the available package types.

**Table 13-1. MC Order Numbers**

Package Type	Operating Temperature Range	MC Order Number
28-Pin Plastic Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HC05RC18P
28-Pin Small Outline Integrated Circuit Package (SOIC)	0 °C to 70 °C	MC68HC05RC18DW
44-Pin Plastic Leaded Chip Carrier (PLCC)	0 °C to 70 °C	MC68HC05RC18FN



## Appendix A. MC68HC05RC9

### A.1 Contents

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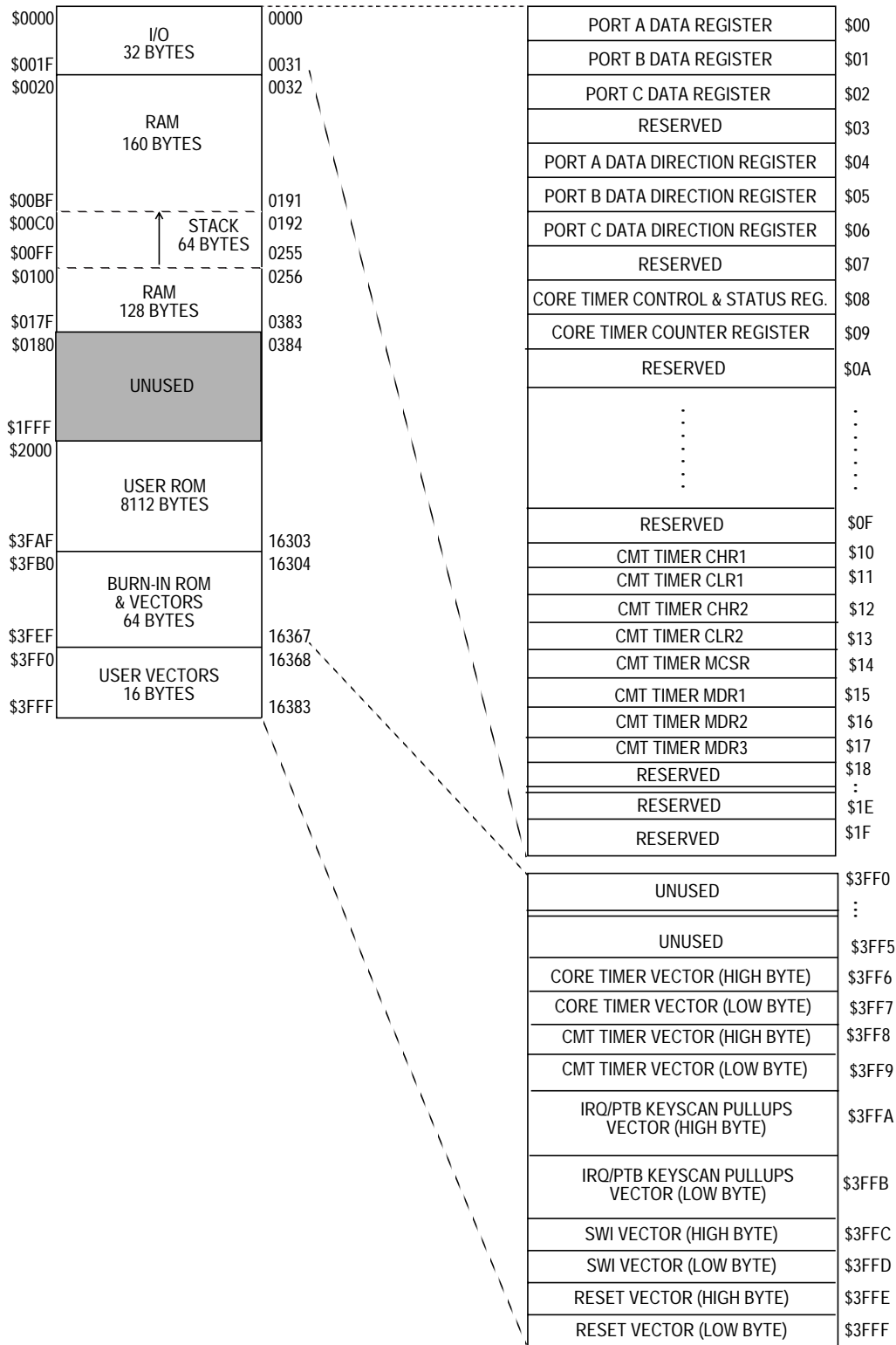
### A.2 Introduction

Appendix A introduces the MC68HC05RC9. The technical data applying to the MC68HC05RC18 applies to the MC68HC05RC9 with the exceptions given in this appendix.

### A.3 Memory Map


Both the MC68HC05RC9 and the MC68HC05RC18 have 16-Kbyte memory maps consisting of user ROM, RAM, burn-in ROM, and input/output (I/O). However, the user ROM for the MC68HC05RC9 consists of only 8112 bytes of ROM.

**Figure A-1** shows the MC68HC05RC9 memory map in user mode.



**Figure A-1. MC68HC05RC9 Memory Map**



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